Introduction to Micro- and Nano-fabrications

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The first transistor: Bell Labs, December 23, 1947

Integrated Circuit Manufacture


Integrated circuit 1998-2000

0.75 micron dielectric features

0.18 micron dielectric features
Moore’s Law Example: Size/complexity

Historical trend and SIA roadmap projections 1994….
Technologies Involved in Micro- and Nano-fabrications
Single crystal silicon ingots are produced with a crystal pulling process called the CZ (Czochralski) method.

Crushed high-purity polycrystalline silicon is doped with elements like boron or phosphorous and melted at 1400° in a quartz crucible surrounded by an inert gas atmosphere of high-purity argon. The melt is cooled to a precise temperature, then a "seed" of single crystal silicon is placed into the melt and slowly rotated as it is "pulled" out.
**Ingot Characterization**

Single crystal silicon ingots are characterized by the orientation of their silicon crystals. Before the ingot is cut into wafers, one or two "flats" are ground into the diameter of the ingot to mark this orientation.

**Wafer Slicing**

After characterization, wafer producers (Komatsu Silicon America, MEMC, Mitsubishi Silicon America) slice the ingot into individual wafers with a precision "ID Saw" (so named because the cutting edge of the blade is on the inside) or a wire saw. You only need the surface of the semiconductor; the thinner the slice the more efficient the process.
**Wafer Polishing**

Next, the wafers are polished in a series of a combination chemical and mechanical polishing processes.

The wafers are held in a hard ceramic chuck using either wax bonding or vacuum and buffed with a slurry of silica powder, DI water and sodium hydroxide.

The polishing process usually involves two or three polishing steps with progressively finer slurry and intermediate cleanings using RO/DI water.
The purpose of EPI growth is to create a layer with different, usually lower, concentration of electrically active dopant on the substrate. For example, an n-type layer on a p-type wafer.
Oxidation Layering.

Oxidation layering produces a thin layer of silicon dioxide, or oxide, on the substrate by exposing the wafer to a mixture of high-purity oxygen and hydrogen at ± 1000°C (1800°F).

Oxide is used to provide insulating and passivation layers and to form transistor gates. Insulating oxide layers are usually about ± 1500 Å. Gate layers are usually between below 200 Å.
**Photoresist Coating.**

Photoresist is a photo-sensitive material applied to the wafer in a liquid state in small quantities. The wafer is spun at ca. 3000 rpm which spreads the "puddle" into a uniform layer between 2 and 200 µm thick.
**Lithographic Exposure.**

A lithographic exposure tool exposes a photoresist coated wafer UV light passing through a reticle which contains the image of a single device layer. Many exposure tools are termed "steppers" because of the "step-and-repeat" action of moving the wafer on its x and y axes to align the reticle with each individual device position. UV light is used because modern semiconductor device features are so small that the actual wavelength of the exposing light is a limiting factor.
**Develop and Bake.**
After exposure, wafers are developed in either an acid or base solution to remove the exposed areas of photoresist. Once the exposed photoresist is removed, the wafer is "soft-baked" at a low temperature to harden the remaining photoresist.
**Acid Etch and Strip.**
Removing selected areas of material from a wafer involves the use of many different types of acid and caustic solutions.

**Spin, Rinse, and Dry.**
Since protecting the wafer surface from damage and contamination is a primary concern, the wafers must be constantly cleaned. Since this is such a frequent and important operation, a special tool called an SRD (or Spin, Rinse and Dryer) is used.
**Ion Implantation:** doping of semiconductor.

Ion Implant is different from other semiconductor processes because it does not create a new layer on the wafer. Instead, ion implant changes the electrical characteristics of precise areas within an existing layer on the wafer.
An ion implanter uses a high-current accelerator tube and steering and focusing magnets to bombard the surface of the wafer with ions of a particular dopant. These dopant ions are implanted into the top layer of the wafer just below the surface, changing the conductivity of a precise region.
Deposition: Chemical Vapor Deposition.

Controlled chemical reactions in the gas phase are used to create insulating, conducting, or semiconducting layers on wafers.

Using nitrogen and hydrogen as carrier gases, CVD can produce a variety of layer types. For example, ammonia and dichlorosilane will produce a silicon nitride layer. Silane and oxygen are used to create silicon dioxide layers.
A variant of CVD called Plasma-Enhanced Chemical Vapor Deposition, or PECVD, uses a gas plasma to lower the temperature required to obtain a chemical reaction and achieve film deposition.
Deposition by Physical Vapor Deposition (PVD).

**Evaporation** uses heat (either an electric filament or an electron beam) and high-vacuum (between $5 \times 10^{-5}$ Torr and $1 \times 10^{-7}$ Torr) to vaporize the metal source.

**Sputtering** uses a cathode to create an argon plasma which bombards the source metal. The dislodged metal molecules are focused by a "lens" of radiation-absorbent material, called a collimator, and deposited in a thin film on the surface of the wafer.
Passivation.

After the final passivation layers are applied, the entire wafer goes through backside prep, which thins the wafer to allow better heat dissipation and removes stress fractures which could cause breakage.
**Test.**

Each finished wafer may contain several hundred actual devices or die. Fabricators such as Hewlett Packard, IBM, Intel, LSI Logic, use automated methods to test each device on the wafer before it is broken into "chips."

A probe tester uses needle-like "probes" to contact the bonding pads on each device and check its operation. Devices that fail the test are marked with colored dye so they won't be carried further into the production process.

**Die Cut.**

After probe test, the wafer is scored and broken into individual die. The marked (non-functional) die are discarded and the functional die passed on into the wire bonding process.
Lead Frame Assembly and Wire Bonding.

Once separated into individual die, the functional devices are attached to a lead frame assembly and aluminum or gold leads are attached via thermal compression or ultrasonic welding. The automated process attaches the ultra-thin wires (about 30 µm in diameter, 1/3 the diameter of a human hair) between each device bonding pad and a connector of the lead frame.
Packaging.

After wire bonding is completed, the packaging is completed by sealing the device into a ceramic or plastic enclosure.
Key of Micro- and Nano-fabrications

Lithography

Photo-lithography

E-beam lithography
Key of Micro- and Nano-fabrications

Lithography

Photo-lithography

E-beam lithography

Equipments
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- Inspection Microscope
- Oxygen Asher
- Focused Ion Beam Mill
- Tube Furnace
- PECVD Tool (Oxide, Nitride)
- Mask Aligner
- Stepper
- E-Beam Lithography
- E-Beam Evaporator
- Thermal Evaporator
Equipments

- Rapid Thermal Annealer/Processor
- Reactive Ion Etcher
- Induction Coupled Plasma Etcher
- Metal Sputtering System
- Surface Profilometer (Dektak)
- Dicing Saw
- Wire Bonder
- Wet Etcher/Cleaner
- Ellipsometer
- Probe Station
Key of Micro- and Nano-fabrications

Lithography

- Photo-lithography
- E-beam lithography

Photo-lithography procedures to fabricate a MOSFET
Major Fabrication Steps in MOS Process Flow

Oxidation (Field oxide)

Photoresist Coating

Mask-Wafer Alignment and Exposure

Exposed Photoresist

Photoresist Develop

Oxide Etch

Photoresist Strip

Oxidation (Gate oxide)

Polysilicon Deposition

Polysilicon Mask and Etch

Ion Implantation

Active Regions

Nitride Deposition

Contact Etch

Metal Deposition and Etch

Used with permission from Advanced Micro Devices
Schematic creation of MOS field effect transistor.
Step 0

The positively doped silicon wafer is first coated with an insulating layer of silicon dioxide (yellow) through chemical vapor deposition or thermal oxidation.
Step 1

An ultraviolet light-sensitive thin layer of photoresist (blue) is applied to the silicon dioxide surface and evenly spread across the wafer.
Step 2

The first mask is placed over the wafer and ultraviolet light is projected onto the mask. Areas of photoresist exposed to the light are hardened and those shielded remain soft.

(Lithography step number 1)
Step 3

The unexposed (and soft) photoresist is removed by washing with a solvent, leaving the hardened resist and underlying silicon dioxide layer intact.
Step 4

The upper layer of the silicon dioxide is removed by etching with hot gasses, leaving only a very thin layer for insulation.
Step 5

The hardened photoresist is removed with a chemical solvent leaving an uneven silicon dioxide surface over the entire wafer.
Step 6

A layer of conducting polysilicon is then deposited onto the silicon dioxide surface using chemical vapor deposition. This material will serve as the transistor's gate.
Step 7

A second layer of photoresist is applied over the polysilicon to prepare the wafer's surface for a second photomask.
Step 8

The second mask is placed over the wafer and ultraviolet light is again projected onto the mask. The areas exposed to the light are hardened.

(Lithography step number 2)
Step 9

The unexposed photoresist is washed away with a solvent, leaving only the T-shaped hardened resist on the wafer.
Step 10

The next step is ion-beam milling (etching) to remove the excess polysilicon and another thin layer of silicon dioxide exposing the silicon wafer's surface.
Step 11

The photoresist is removed with solvent leaving a ridge of polysilicon (the transistor's gate), which rises above the silicon wells.
Step 12

Chemical doping implants phosphorous (green) deep within the silicon wells surrounded by the silicon dioxide and polysilicon layers to produce positively doped silicon.
Step 13

A second layer of silicon dioxide is applied to provide insulation of the basic transistor structure from metal contacts to be applied later.
Step 14

A third film of photoresist is added to prepare the formation of vertical shafts (vias) that will contain metal contacts for the polysilicon and the wells.
Step 15

The third mask is illuminated with ultraviolet light, hardening the photoresist everywhere with the exception of small black rectangles that will become shafts.

(Lithography step number 3)
Step 16

Removal of the soft photoresist with solvent exposes three areas of exposed silicon dioxide that mark the planned shafts.
Step 17

The wafer is next etched again to remove silicon dioxide and exposing the positively doped silicon and the polysilicon gate.
Step 18

The remaining photoresist is then washed away with solvent. The positively doped silicon areas (green) will serve as the source and the drain.
Step 19

The wafer is then sputter-coated with aluminum that fills the shafts and evenly coats the wafer's surface to provide electrical contacts.
Step 20

A fourth layer of photoresist is applied to the wafer to prepare the transistor for its final mask, which will produce the pattern for the aluminum "wiring".
Step 21

Ultraviolet light shining through the metallization mask hardens the photoresist covering the aluminum, which will carry current to and from the transistor.

(Lithography step number 4)
Step 22

The unexposed photoresist is removed with solvent, exposing many bare regions of aluminum that will be removed next.
**Step 23**

A final etching step removes exposed aluminum leaving only the metal necessary to make contacts in the shafts and connectors on the surface.
Step 24

The last resist is washed away with solvent and the transistor is finished, along with millions of its neighbors on the wafer.
Knowledge on micro- and nano-fabrication in more details

ECE 541/ME 541
Microelectronic Fabrication Techniques

Spring Semester