Text Book:

Silicon VLSI Technology
Fundamentals, Practice and Modeling
Authors: J. D. Plummer, M. D. Deal, and P. B. Griffin
Chapter 4

- A three tiered approach to control unwanted impurities in silicon
  - Clean Rooms
    - Minimize particles in the environment
  - Wafer Cleaning
    - Minimize particles on the wafers
  - Gettering
    - Minimize the effect of particles in the wafer
Over the next several weeks, we’ll study front end processes individually.

Cleaning belongs to front end processes and is an important part of fabrication.

Defect and Impurities

- Importance of unwanted impurities increases with shrinking geometries of devices.
- 75% of the yield loss is due to defects caused by particles (1/2 of the minimum feature size).
- Wafer localized light scatterers (LLS) is a starting wafer test.
- Crystal originated (45-150nm) particles (COP) ~1,000Å~void with SiOx -> affect gate oxide integrity (GOI).
- -> anneal in H2 -> oxide decomposes and surface reconstructs! & oxide precipitates from deep depth in Si.

### Table 4-1

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<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Minimum Feature Size</td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td>Wafer Diameter (mm)</td>
<td>200</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>450</td>
<td>450</td>
</tr>
<tr>
<td>DRAM Bits/Chip</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
<td>256G</td>
</tr>
<tr>
<td>DRAM Chip Size (mm²)</td>
<td>280</td>
<td>400</td>
<td>560</td>
<td>790</td>
<td>1120</td>
<td>1580</td>
</tr>
<tr>
<td>Microprocessor Transistors/chip</td>
<td>11M</td>
<td>21M</td>
<td>76M</td>
<td>200M</td>
<td>520M</td>
<td>1.40B</td>
</tr>
<tr>
<td>Maximum Wiring Levels</td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
<td>9</td>
</tr>
<tr>
<td>Minimum Mask Count</td>
<td>22</td>
<td>22/24</td>
<td>24</td>
<td>24/26</td>
<td>26/28</td>
<td>28</td>
</tr>
<tr>
<td>Critical Defect Size</td>
<td>125</td>
<td>90</td>
<td>65</td>
<td>50</td>
<td>35</td>
<td>25</td>
</tr>
<tr>
<td>Starting Wafer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total LLS (cm²)</td>
<td>0.60</td>
<td>0.29</td>
<td>0.14</td>
<td>0.06</td>
<td>0.03</td>
<td>0.015</td>
</tr>
<tr>
<td>DRAM GOI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Defect Density (cm⁻²)</td>
<td>0.06</td>
<td>0.03</td>
<td>0.014</td>
<td>0.006</td>
<td>0.003</td>
<td>0.001</td>
</tr>
<tr>
<td>Logic GOI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Defect Density (cm⁻²)</td>
<td>0.15</td>
<td>0.15</td>
<td>0.08</td>
<td>0.05</td>
<td>0.04</td>
<td>0.03</td>
</tr>
<tr>
<td>Starting Wafer</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Total Bulk Fe (cm⁻³)</td>
<td>3 x 10¹⁰</td>
<td>1 x 10¹⁰</td>
<td>Under 1 x 10¹⁰</td>
<td>Under 1 x 10¹⁰</td>
<td>Under 1 x 10¹⁰</td>
<td>Under 1 x 10¹⁰</td>
</tr>
<tr>
<td>Critical Metals on Wafer Surface After Cleaning (cm⁻²)</td>
<td>5 x 10⁹</td>
<td>4 x 10⁹</td>
<td>2 x 10⁹</td>
<td>1 x 10⁹</td>
<td>&lt; 10⁹</td>
<td>&lt; 10⁹</td>
</tr>
<tr>
<td>Starting Material Recombination Lifetime (μsec)</td>
<td>≥ 300</td>
<td>≥ 325</td>
<td>≥ 325</td>
<td>≥ 325</td>
<td>≥ 450</td>
<td>≥ 450</td>
</tr>
</tbody>
</table>

Yield > 90% at the end requires > 99% @ each step
Wafer Cleaning

• Surface films and doped regions must not be significantly attacked.
• Photoresist strip and particle removal typical
• Room air and process equipment delivered particles
  – Significant elements that cause severe problems in silicon include: organics, metals (Fe, Au, Cu, etc.) and alkali ions (Na, K, etc.)
Example Sensitivity

• Example #1: MOS transistor gate threshold shift

MOS $V_{TH}$ is given by

$$V_{TH} = V_{FB} + 2\phi_f + \frac{\sqrt{2\varepsilon_S qN_A (2\phi_f)}}{C_O} + \frac{qQ_M}{C_O}$$  (1)

- $Q_M$ is the mobile charge density (number of charges per cm$^2$) of Na$^+$ and K$^+$ in the gate oxide.

If $t_{ox} = 10$ nm, then a 0.1 volt $V_{th}$ shift can be caused by

$Q_M = 6.5 \times 10^{11}$ cm$^{-2}$ (< 0.1% monolayer or 10 ppm in the oxide).

- Prevented MOS technologies initially from being important commercially!
Example Sensitivity

- Example #2: MOS DRAM
  - Storage of charge based on minimal charge leakage in time.
    - Refresh required to maintain charges after a technology defined period of time.
    - Dominated by Shockley, Reed Hall (SRH) recombination (intermediate impurity related energy levels).
      - $\sigma$ is the trap cross sectional area, $(10^{-15}\text{cm}^{-2}) \, v_{th}$ is the minority carrier thermal velocity $(10^7 \text{ cm/sec})$, and $N_t$ is the density of traps.
      - Deep-level traps (Cu, Fe, Au etc.) Pile up at the surface where the devices are located.

- Refresh time of several msec requires a generation lifetime of

\[
\tau_R = \frac{1}{\sigma \cdot v_{th} \cdot N_t} \approx 100 \mu\text{sec} \quad (2)
\]

- This requires $N_t \approx 10^{12} \text{ cm}^{-3}$ or $\approx 0.02 \text{ ppb}$ (see text).
Example: The Role of Surface Cleaning in Processing

Residual contaminants, layers affect kinetics of processes.

Surface effects are very important (MORE) in scaled down devices.
## 2003 ITRS Front End Processes

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology Node (half pitch)</strong></td>
<td>250 nm</td>
<td>180 nm</td>
<td>130 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
<td>18 nm</td>
</tr>
<tr>
<td><strong>MPU Printed Gate Length</strong></td>
<td>100 nm</td>
<td>70 nm</td>
<td>53 nm</td>
<td>35 nm</td>
<td>25 nm</td>
<td>18 nm</td>
<td>13 nm</td>
<td>10 nm</td>
<td></td>
</tr>
<tr>
<td><strong>DRAM Bits/Chip (Sampling)</strong></td>
<td>256M</td>
<td>512M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>32G</td>
<td>64G</td>
<td>128G</td>
<td>128G</td>
</tr>
<tr>
<td><strong>MPU Transistors/Chip (x10^6)</strong></td>
<td>550</td>
<td>1100</td>
<td>2200</td>
<td>4400</td>
<td>8800</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Critical Defect Size</strong></td>
<td>125 nm</td>
<td>90 nm</td>
<td>90 nm</td>
<td>90 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>45 nm</td>
<td></td>
</tr>
<tr>
<td><strong>Starting Wafer Particles (cm^-2)</strong></td>
<td>&lt;0.35</td>
<td>&lt;0.18</td>
<td>&lt;0.09</td>
<td>&lt;0.09</td>
<td>&lt;0.05</td>
<td>&lt;0.05</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Starting Wafer Total Bulk Fe (cm^-3)</strong></td>
<td>3x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
</tr>
<tr>
<td><strong>Metal Atoms on Wafer Surface After Cleaning (cm^-2)</strong></td>
<td>5x10^9</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
<td>1x10^10</td>
</tr>
<tr>
<td><strong>Particles on Wafer Surface After Cleaning (#/wafer)</strong></td>
<td>75</td>
<td>80</td>
<td>86</td>
<td>195</td>
<td>106</td>
<td>168</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## ITRS 2007 Ed. Front End Processes

### Table FEP2a

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM Pitch (nm)</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
<td>28</td>
<td>25</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) Pitch (nm)</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
<td>28</td>
<td>25</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>25</td>
<td>23</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>DRAM Total Chip Area (mm²)</td>
<td>93</td>
<td>74</td>
<td>59</td>
<td>93</td>
<td>74</td>
<td>59</td>
<td>93</td>
<td>74</td>
<td>59</td>
</tr>
<tr>
<td>DRAM Active Transistor Area (mm²)</td>
<td>29.6</td>
<td>23.1</td>
<td>18.2</td>
<td>29.1</td>
<td>23.1</td>
<td>18.3</td>
<td>29.1</td>
<td>23.1</td>
<td>18.3</td>
</tr>
<tr>
<td>MPU High-Performance Total Chip Area (mm²)</td>
<td>310</td>
<td>246</td>
<td>195</td>
<td>310</td>
<td>246</td>
<td>195</td>
<td>310</td>
<td>246</td>
<td>195</td>
</tr>
<tr>
<td>MPU High Performance Active Transistor Area (mm²)</td>
<td>31.7</td>
<td>25.1</td>
<td>20.0</td>
<td>31.7</td>
<td>25.1</td>
<td>20.0</td>
<td>31.7</td>
<td>25.1</td>
<td>20.0</td>
</tr>
</tbody>
</table>

**General Characteristics * (99% Chip Yield)**

<table>
<thead>
<tr>
<th>Maximum Substrate Diameter (mm)—High-volume Production (&gt;20K wafer starts per month)**</th>
<th>300</th>
<th>300</th>
<th>300</th>
<th>300</th>
<th>300</th>
<th>450</th>
<th>450</th>
<th>450</th>
<th>450</th>
</tr>
</thead>
<tbody>
<tr>
<td>Edge exclusion (mm)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
</tr>
<tr>
<td>Front surface particle size (nm), latex sphere equivalent (Å)</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
<td>&gt;65</td>
</tr>
<tr>
<td>Particles (cm⁻²)</td>
<td>≤0.32</td>
<td>≤0.30</td>
<td>≤0.30</td>
<td>≤0.15</td>
<td>≤0.15</td>
<td>≤0.15</td>
<td>≤0.15</td>
<td>≤0.16</td>
<td>≤0.16</td>
</tr>
<tr>
<td>Particles (#/μm²)</td>
<td>≤218</td>
<td>≤209</td>
<td>≤205</td>
<td>≤105</td>
<td>≤105</td>
<td>≤498</td>
<td>≤249</td>
<td>≤249</td>
<td>≤492</td>
</tr>
<tr>
<td>Site flatness (nm), SFQR 26mm x 8 mm Site Size</td>
<td>≤65</td>
<td>≤57</td>
<td>≤50</td>
<td>≤45</td>
<td>≤40</td>
<td>≤36</td>
<td>≤32</td>
<td>≤28</td>
<td>≤25</td>
</tr>
<tr>
<td>Nanotopography, p-, n-, 2 mm dia. analysis area (l)</td>
<td>≤16</td>
<td>≤14</td>
<td>≤13</td>
<td>≤11</td>
<td>≤10</td>
<td>≤9</td>
<td>≤8</td>
<td>≤7</td>
<td>≤6</td>
</tr>
<tr>
<td>Epitaxial Wafer * (99% Chip Yield)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Large structural epi defects (DRAM) (cm⁻²) (B)</td>
<td>≤0.011</td>
<td>≤0.014</td>
<td>≤0.017</td>
<td>≤0.011</td>
<td>≤0.014</td>
<td>≤0.017</td>
<td>≤0.011</td>
<td>≤0.014</td>
<td>≤0.017</td>
</tr>
<tr>
<td>Large structural epi defects (MPU) (cm⁻²) (B)</td>
<td>≤0.003</td>
<td>≤0.004</td>
<td>≤0.005</td>
<td>≤0.003</td>
<td>≤0.004</td>
<td>≤0.005</td>
<td>≤0.003</td>
<td>≤0.004</td>
<td>≤0.005</td>
</tr>
<tr>
<td>Small structural epi defects (DRAM) (cm⁻²) (C)</td>
<td>≤0.022</td>
<td>≤0.027</td>
<td>≤0.034</td>
<td>≤0.022</td>
<td>≤0.027</td>
<td>≤0.034</td>
<td>≤0.022</td>
<td>≤0.027</td>
<td>≤0.034</td>
</tr>
<tr>
<td>Small structural epi defects (MPU) (cm⁻²) (C)</td>
<td>≤0.006</td>
<td>≤0.008</td>
<td>≤0.010</td>
<td>≤0.006</td>
<td>≤0.008</td>
<td>≤0.010</td>
<td>≤0.006</td>
<td>≤0.008</td>
<td>≤0.010</td>
</tr>
</tbody>
</table>
Clean Factories – Wafer Fab Facility

• The wafer fabrication area “Clean Rooms” must particle free.
  – Sources of particles
    • Air (normal presence of particles) and Water
    • Machinery – particularly due to friction, metals
    • People – 5 to 10 million particles per minute, organic
    • Supplies – brought in to room for use
    • Processing
  – Rooms and People
    • Clean room limited access, finger wall machine access
    • Bunny suits, gloves, air showers, covered faces/facemask
    • Glove box and robots
  – Air handling
    • Positive air pressure, HEPA filters
Stanford’s CIS Clean Room

- The 10,500 square feet clean room is vibration-isolated from the rest of the building. Support equipment, such as chilled water, vacuum pumps, air compressors, and acid waste neutralizers, are located in the basement. Corrosive and toxic gases are in a monitored gas area. Liquid gas storage tanks, emergency power generators, and a de-ionized water plant are outdoors.

- Every 8 seconds, the entire air volume of this room is circulated out to large air ducts, like the meter-wide duct just behind the glass. From there the air flows up to the third floor, down through filters on the second floor, and then back into the clean room through the ceiling.

- People inside the room wear bunny suits to minimize the release of human particles into the air. The result is that each cubic foot of air has fewer than 100 particles of size 500 nanometers (Class 100), much cleaner than the air in a hospital operating room.

- [http://www-cis.stanford.edu/~marigros/CleanRoom.html](http://www-cis.stanford.edu/~marigros/CleanRoom.html)
- [http://snf.stanford.edu/Education/VirtualTour.html](http://snf.stanford.edu/Education/VirtualTour.html)
Level 1 Contamination Reduction: Clean Factories

- Air quality is measured by the “class” of the facility.
  - Less than X total particles greater than 0.5 um per cubic foot of air.

Factory environment is cleaned by:
- HEPA filters (99.07% eff.)
- Air recirculation (laminar >50 cm/sec)
- Bunny suits for workers
- Filtration of chemicals and gases
- Manufacturing protocols

(Photo courtesy of Stanford Nanofabrication Facility.)
Wafer Cleaning

- Remove particles, films such as photoresist, and any other trace contaminants
- Distinct processes
  - Silicon wafer clean (frontend processes)
  - Post metalization clean (backend processes)
- Frontend Wafer Cleaning based on RCA process
  - RCA was originally the Radio Corporation of America
  - Werner Kern developed the basic procedure in 1965 while working for RCA.
- The RCA clean involves the following:
  1. Removal of the organic contaminants (Organic Clean)
  2. Removal of thin oxide layer (Oxide Strip)
  3. Removal of ionic contamination (Ionic Clean)
The RCA Clean

- The first step (called SC-1, where SC stands for Standard Clean) is performed with a 1:1:5 solution of NH$_4$OH + H$_2$O$_2$ + H$_2$O at 70º to 80º C for 10 minutes.
  - This treatment oxidizes organic films and complexes Group IB and IIB metals as well as Au, Ag, Cu, Ni, Zn, Cd, Co, and Cr. The solution dissolves and regrows a thin native oxide layer on the silicon.
- The next step is a short immersion in a 1:50 solution of HF + H$_2$O at 25º C
  - Remove the thin oxide layer and some fraction of ionic contaminants.
- Perform a DI rinse.
- The next step (called SC-2) is performed with a 1:1:6 solution of HCl + H$_2$O$_2$ + H$_2$O at 70º to 80º C for 10 minutes.
  - This treatment removes alkali ions and cations (Al, Fe, Mg) that form NH$_4$OH insoluble hydroxides in solutions like SC-1. In SC-2 they form soluble complexes. This solution also completes the removal of metal contaminants.
- Perform a DI rinse.
Level 2 Contamination Reduction: Wafer Cleaning

- Organic Clean
- RCA clean is “standard process” used to remove organics, heavy metals and alkali ions.
- Ultrasonic agitation is used to dislodge particles.
De-Ionized (DI) Water

• Clean water for silicon processing

• DI Water conductivity example:

DI water is necessary: \( H_2O \leftrightarrow H^+ + OH^- \) with \( [H^+] = [OH^-] = 6 \times 10^{-13} \text{cm}^{-3} \)

Diffusivity of: \( H^+ \approx 9.3 \times 10^{-5} \text{cm}^2\text{s}^{-1} \)

of: \( OH^- \approx 5.3 \times 10^{-5} \text{cm}^2\text{s}^{-1} \)

\[
\rho = \frac{1}{q([H^+]\mu_{H^+} + [OH^-]\mu_{OH^-})} = 18.5 \text{M} \Omega \text{cm}
\]

Distilled water is typically 10 uS/cm or 0.1 M\( \Omega \) cm
Gettering

• Removing trace elements from active transistor locations by causing them to combine with defects in the silicon.
  – Active devices cover a very small portion of the silicon volume, typically near one surface.
  – Metals and alkali ions have very high diffusivity.
  – They tend to be easily captured either in regions with mechanical defects or in regions which chemically trap them.

• For the alkali ions, gettering generally uses dielectric layers on the topside (PSG or barrier Si3N4 layers).

• For metal ions, gettering generally uses traps on the wafer backside (extrinsic) or in the wafer bulk (intrinsic).
Level 3 Contamination Reduction: Gettering

Elements for gettering:
- Alkali Ions
- Metals
Gettering

- **Steps:**
  1. Free elements from current sites, making them mobile
  2. Diffuse through silicon to desired sites
  3. Become trapped.

- **Aalkali ions:** dielectric layers on the topside (PSG or barrier Si3N4 layers).
- **Heavy metal ions:** traps on the wafer backside (extrinsic) or in the wafer bulk (intrinsic).
Gettering

- Diffusivity of various elements
  - Diffuse as interstitials (they don’t easily fit in the lattice) (through wafer during normal dopant drive-in)
  - Dopants diffuse as a substitution
• “Trap” sites can be created by SiO₂ precipitates (intrinsic gettering), or by backside damage (extrinsic gettering).

• In intrinsic gettering, CZ silicon is used and SiO₂ precipitates are formed in the wafer bulk through temperature cycling at the start of the process.
Intrinsic Gettering: Oxide Precipitates

Precipitates (size) grow @ high T

Density of nucleation sites grow @ low T

The largest & the most dense defects -> the most efficient gettering

Surface (top) has few defects.
MEASUREMENT METHODS
Measurement Methods

• Clean factories = particle control
  – Detect concentrations < 10/wafer of particles smaller than 0.1 µm

• Unpatterened wafers (blank)
  – Count particles in microscope
  – Laser scanning systems → maps of particles down to ≈ 0.2 µm
    (see MEMC video on laser inspection from Chapter 3)

• Patterned wafers
  – Optical system compares a die with a “known good reference”
    die (adjacent die, chip design - its appearance)
  – Image processing identifies defects (SEM)
  – Test structure (not in high volume manufacturing)
Test Structures

Resistance

Capacitance

Trapped charge

$Q_T \rightarrow V_{TH}$ change

Dielectric breakdown due to particles, metals etc.

**Figure 4-14** Layout (top view) of a typical electrical test structure designed to detect defects in an interconnect layer. Typical open and short defects are illustrated.

**Figure 4-15** MOS capacitor test structure. The voltage applied to the gate is ramped up until significant current flows through the gate dielectric. The electric field at which this breakdown occurs is plotted on the right.
Monitoring the Wafer Cleaning Efficiency

Concentrations of impurities determined by surface analysis

- Excite
- Identify (unique atomic signature)
- Count concentrations

![Diagram showing surface analysis techniques](image)

**Figure 4-16** Surface analysis techniques used to identify and quantify contamination in IC manufacturing.

- Primary beam – e⁻: good lateral resolution
- Detected beam – e⁻: good depth resolution and surface sensitivity
- X-ray: poor depth resolution and poor surface sensitivity
- Ions (SIMS): excellent
- Ions (RBS): good depth resolution, reasonable sensitivity (0.1 atomic%)

**Rutherford Back-scattering**

**Secondary Ion Mass Spectrometry**: O⁺ or Cs⁺ sputtering and mass analyses

**SUMMARY**

- **Secondary Ion Mass Spectrometry (SIMS)**
  - RBS: good depth resolution, reasonable sensitivity (0.1 atomic%)

- **Rutherford Back-scattering**
  - Good depth resolution, reasonable sensitivity (0.1 atomic%)

- **Secondary Ion Mass Spectrometry (SIMS)**
  - Excellent depth resolution

**REFERENCES**

Electron Beam Emissions (1)

Inelastic collision with target electrons, which are then emitted from the solid (as in SEM).

Elastic collision of incoming electrons with atoms (reflected back) ~ the same energy as for the incoming electrons.

Figure 4-17: Energy distribution of electrons emitted from a solid under electron bombardment.

~ 5 eV
Electron Beam Emissions (2)

If X-Ray is at the input:
- el. Emitted = X-ray Photoelectron Spectroscopy (XPS)
- X-ray emitted = X-ray Fluorescence (XRF)

XPS usually more dominant for lighter elements, XRF for heavier elements.

AES scheme is for lighter elements (Z=33 as is crossover between Auger AES and X-Ray/XES)

The core electron energy levels

Events where a core electron is kicked out:
- 1. Secondary electron
- 2. Secondary electron
- 3. Ejected Auger electron

Figure 4-18 Band diagram representation of some of the processes used in surface analytical methods.
Monitoring of Gettering Through Device Properties and Dielectric

p – n leakage, refresh time DRAM junction and dielectric breakdown, β of n-p-n emission↔capture

Material properties: \( \tau_G(\gg \tau_R) \) in the bulk and on the surface

**Photoconductive Decay** Measurements

\[ \Delta n = g_{op} \tau_G \]

- Carriers are generated due to light
- Decrease resistivity
- Recombine

\[ \Delta n(t) = \Delta n(0) \exp\left(-t / \tau_R\right) \]
Carrier Generation Lifetime

\[ \tau_G = 10 \left( \frac{N_A}{n_i} \right) \tau_G \]

**Zerbst technique:**

\[ \frac{d}{dt} \left( \frac{C_{ox}}{C} \right)^2 \rightarrow \tau_G \]

\[ \frac{d}{dt} \left( \frac{C_{ox}}{C} \right)^2 \rightarrow s \quad \text{if plotted vs.} \ (C_{min}/C)-1 \]

\( s = f(N_{STB}, \sigma) \)

\( \sigma = \text{Capture cross section} \)

**Figure 4-19** MOS CV measurement to extract the carrier generation lifetime. At \( t = \) deep depletion. As carriers inversion shrinks.

Deep Depletion - Return to Inversion via Carrier Generation (measure \( \tau_G \)) and surface recombination (\( s \))

SILICON VLSI TECHNOLOGY
Fundamentals, Practice and Modeling
By Plummer, Deal & Griffin

© 2000 by Prentice Hall
Upper Saddle River NJ
**Lifetime Measurements: Open Circuit Voltage Decay**

Given a circuit with a diode switched from ON to OFF when carriers recombine, the voltage decay can be described by the equation:

\[ V_D(t) = V_D(0) - kT \ln(\text{erfc} \left( \frac{t}{\tau_R} \right)) \]

where:
- \( V_D(0) \) is the initial voltage
- \( kT \) is the thermal voltage
- \( \text{erfc} \) is the complementary error function
- \( \tau_R = \frac{kT}{q} \frac{dV_D}{dt} \)

For \( t/\tau > 4 \), the voltage decay is approximately:

\[ V_D(t) \approx 0.7V \]

Diode switched from ON to OFF when carriers recombine.

Measurements include surface and bulk recombination.

**Figure 4-20** Diode open circuit voltage decay to extract the carrier recombination lifetime. The switch is opened at \( t = 0 \). The diode voltage decays due to carrier recombination.

Use also DLTS:
- Identifies traps (\( E_t \)) and concentrations
- Thermal or photoexcitation processes in voltage modulable space-charge region
- (Schottky Diode, p-n junction, MOS Capacitor)
- Measured: capacitance, currents or conductance
Deep Level Transient Spectroscopy

• An experimental tool for studying electrically active defects (known as charge carrier traps) in semiconductors.
  – DLTS enables to establish fundamental defect parameters and measure their concentration in the material.
  – Some of the parameters are considered as defect “finger prints” used for their identifications and analysis.
  – identifies traps (Et) and concentrations

• Thermal or photoexcitation processes in voltage modulable space-charge region (Schottky Diode, p-n junction, MOS Capacitor)
  – Measured: capacitance, currents or conductance
MODELING
Models and Simulation Goal

Computer Integrated Manufacturing (CIM)

- Tools to monitor and control machines, to maintain recipes, to control wafer throughput, and to improve operating efficiency (i.e. higher yields)
- Higher initial yields and shorter time to maturity.

Table 4-2  Semiconductor industry projected progress and the implications of this progress for chip yield and manufacturing yield ramp-up [4.1].

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Feature Size (nm)</td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td>Wafer Diameter (mm)</td>
<td>200</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>450</td>
<td>450</td>
</tr>
<tr>
<td>DRAM Bits/Chip</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
<td>256G</td>
</tr>
<tr>
<td>Initial Yield Level (%)</td>
<td>25</td>
<td>50</td>
<td>80</td>
<td>85</td>
<td>88</td>
<td>90</td>
</tr>
<tr>
<td>Time to Mature Yield Level (years)</td>
<td>4</td>
<td>3</td>
<td>1</td>
<td>0.8</td>
<td>0.6</td>
<td>0.5</td>
</tr>
</tbody>
</table>
Contamination and Yield

- ≈ 75% of yield loss in modern VLSI fabs is due to particle contamination.
- Yield models depend on information about the distribution of particles.
- Particles on the order of 0.1 - 0.3 µm are the most troublesome:
  - larger particles precipitate easily
  - smaller ones coagulate into larger particles
Contamination and Yield Model

• Yields are described by Poisson statistics in the simplest case.

\[ Y = \exp^{-A_C D_O} \]

where \( A_C \) is the critical area and \( D_O \) the defect density.

• If some fraction of the wafer, \( G \), always produces zero yields (near the edge of the wafer) this is modified as

\[ Y = (1 - G) \cdot \exp^{-A_C D_O} \]

• This model assumes independent randomly distributed defects and often under predicts yields.
Alternate Models

- Use of negative binomial statistics eliminates these assumptions and is more accurate.
  
  - where C is a measure of the particle spatial distribution (clustering factor).

\[ Y = \frac{1}{\left(1 + \frac{A_c D_o}{C}\right)^C} \]
Negative Binomial Yield for C=2

- Vertical lines are estimated chip sizes (from the ITRS).
- Note that defect densities will need to be extremely small in the future to achieve the high yields required for economic IC manufacturing.
- (See particle defect densities on Table 4-1.)
Overall Yield

• The total wafer yield must be the product of the yields for each process step.

\[
Y = \prod_{i=1}^{\text{levels}} \left( 1 + \frac{A_{Ci} D_{Oi}}{C_i} \right)^{-C_i}
\]

• Note that previous curves refer to chip yield
  – Table 4-1 and Figures 4-22 and 4-23
Modeling Wafer Cleaning

• Cleaning involves removing particles, organics (photoresist) and metals from wafer surfaces.
  – Particles are largely removed by ultrasonic agitation during cleaning.
  – Organics like photoresists are removed in an O₂ plasma or in H₂SO₄/H₂O₂ solutions.
  – The “RCA clean” is used to remove metals and any remaining organics.

• Metal cleaning can be understood in terms of:
  – Convert metal into ions soluble in the cleaning solution
    • Oxidation: the process that removes electrons from an atom (→)
    • Reduction: the process that gains and electron (←)

\[
\text{Si} + 2\text{H}_2\text{O} \leftrightarrow \text{SiO}_2 + 4\text{H}^+ + 4\text{e}^- \quad (5)
\]

\[
\text{M} \leftrightarrow \text{M}^{z+} + ze^- \quad (6)
\]
Modeling Wafer Cleaning

\[ Si + 2H_2O \leftrightarrow SiO_2 + 4H^+ + 4e^- \quad (5) \]
\[ M \leftrightarrow M^{z+} + ze^- \quad (6) \]
\[ 2H_2O \leftrightarrow H_2O_2 + 2H^+ + 2e^- \quad (7) \]

- If we have a water solution with a Si wafer and metal atoms and ions, the stronger reaction will dominate.
- Generally (7) is driven to the left and (5) and (6) to the right so that SiO\(_2\) is formed and M\(^{z+}\) is a solution soluble ion.
- Good cleaning solutions drive (6) to the right since M\(^{z+}\) is soluble and will be desorbed from the wafer surface.

- No model exists, but there is a general understanding of the chemistry.
**Oxidation-Reduction Reactions**

<table>
<thead>
<tr>
<th>Oxidant/ Reductant</th>
<th>Standard Oxidation Potential (volts)</th>
<th>Oxidation-Reduction Reaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mn(^{2+})/Mn</td>
<td>1.05</td>
<td>Mn $\leftrightarrow$ Mn(^{2+}) + 2e(^-)</td>
</tr>
<tr>
<td>SiO(_2)/Si</td>
<td>0.84</td>
<td>Si + 2H(_2)O $\leftrightarrow$ SiO(_2) + 4H(^+) + 4e(^-)</td>
</tr>
<tr>
<td>Cr(^{3+})/Cr</td>
<td>0.71</td>
<td>Cr $\leftrightarrow$ Cr(^{3+}) + 3e(^-)</td>
</tr>
<tr>
<td>Ni(^{2+})/Ni</td>
<td>0.25</td>
<td>Ni $\leftrightarrow$ Ni(^{2+}) + 2e(^-)</td>
</tr>
<tr>
<td>Fe(^{3+})/Fe</td>
<td>0.17</td>
<td>Fe $\leftrightarrow$ Fe(^{3+}) + 3e(^-)</td>
</tr>
<tr>
<td>H(_2)SO(_4)/H(_2)SO(_3)</td>
<td>-0.20</td>
<td>H(_2)O + H(_2)SO(_3) $\leftrightarrow$ H(_2)SO(_4) + 2H(^+) + 2e(^-)</td>
</tr>
<tr>
<td>Cu(^{2+})/Cu</td>
<td>-0.34</td>
<td>Cu $\leftrightarrow$ Cu(^{2+}) + 2e(^-)</td>
</tr>
<tr>
<td>O(_2)/H(_2)O</td>
<td>-1.23</td>
<td>2H(_2)O $\leftrightarrow$ O(_2) + 4H(^+) + 2e(^-)</td>
</tr>
<tr>
<td>Au(^{3+})/Au</td>
<td>-1.42</td>
<td>Au $\leftrightarrow$ Au(^{3+}) + 3e(^-)</td>
</tr>
<tr>
<td>H(_2)O(_2)/H(_2)O</td>
<td>-1.77</td>
<td>2H(_2)O $\leftrightarrow$ H(_2)O(_2) + 2H(^+) + 2e(^-)</td>
</tr>
<tr>
<td>O(_3)/O(_2)</td>
<td>-2.07</td>
<td>O(_2) + H(_2)O $\leftrightarrow$ O(_3) + 2H(^+) + 2e(^-)</td>
</tr>
</tbody>
</table>

- The strongest oxidants are at the bottom (H\(_2\)O\(_2\) and O\(_3\)). These reactions go to the left grabbing e\(^-\), dominating, and forcing (6) to the right.
- Fundamentally the RCA clean works by using H\(_2\)O\(_2\) as a strong oxidant.
Modeling Gettering

- Gettering consists of
  1. Making metal atoms mobile.
  2. Migration of these atoms to trapping sites.
  3. Trapping of atoms.

- Step 1 generally happens by “kicking-out” the substitutional atom into an interstitial site. One possible reaction is:

\[
\text{Au}_S + I \leftrightarrow \text{Au}_i
\]

- Step 2 usually happens easily once the metal is interstitial since most metals diffuse rapidly in this form.

- Step 3 happens because heavy metals segregate preferentially to damaged regions or to N⁺ regions or pair with effective getters like P (AuP pairs).
**Gettering**

All metal atoms mobile ($D_{Mi} > D_{Ms}$ 10x)

Except of Ti, Mo, etc.

$D_M \gg D_{Dopants}$

Sol. Sol. $M_i > M_S$ (Cu, Ni)
Sol. Sol. $M_i < M_S$ (Au, Pt)

$Au_S + I \leftrightarrow Au_i$ kick-out mechanism, then getter

$Au_s \leftrightarrow Au_i + V$ dissociative or Frank-Turnbull mech.

I increase improves gettering of Au

V increase hinders gettering

Ex. P diffusion, Ion Implant=damage, intrinsic gettering ($=I \uparrow$)
Metal Diffusion to the Gettering Sites

Initial constant concentration

Time increase

Au diffuses to the wafer back side and is trapped

**Figure 4-25** General shape of Au outdiffusion profiles if simple outdiffusion dominates the gettering process. Starting with a flat profile ($10^{15}$ cm$^{-3}$), the concentration drops off with time through the wafer as the Au diffuses to the back surface (left side). This simulation was done with Silvaco’s SSUPREM IV, a process simulator we will discuss in more detail in later chapters.

**Figure 4-26** Experimental 1000°C Au outdiffusion profiles during gettering to the wafer backside. (After [4.31].)
Trapping the Metal Atoms at the Gettering Sites (1)

- Trapped by: ion implantation, P diffusion, laser damage, poly-Si films, mechanical damage, etc. But HOW?

- Physical damage -> metal trapped at defect sites; binding energy $E_g$ depends on $T$;

$$\text{Fraction Bound} = (1 - K_1 \exp^{E_g/kT})$$

- Segregation, related to solubility in the silicon perfect crystal and in the gettering region

$$C_{\text{Au, Si}} = N_{\text{Si}} \exp(-E_{A1}/kT) \quad \text{in silicon region}$$

$$C_{\text{Au, G}} = N_{\text{G}} \exp(-E_{A2}/kT) \quad \text{in gettering region}$$

- The segregation coefficient is defined as

$$k_0 = (C_{\text{Au, G}} + C_{\text{Au, Si}}) / C_{\text{Au, Si}} = 1 + K_2 \exp[-(E_{A1} - E_{A2})/kT]$$

For the case of phosphorous

$$k_0 = 1 + N_{\text{G}}/5 \times 10^{22} \exp(0.82 \text{eV}/kT) \quad \text{(fraction of Au bound in gettering)}$$
Trapping the Metal Atoms at the Gettering Sites (2)

- Enhances sol.sol by high dopant concentrations: in “n” Au=acceptor, “p” - Au=donor
  \[ \text{Au}^+ + e^- \leftrightarrow \text{Au}^-, \ K_{eq} = \frac{[\text{Au}^-]}{[\text{Au}][e^-]} = \text{constant} \]
  \[ \frac{[\text{Au}^-]}{[\text{Au}]}n_i = \frac{[\text{Au}^-]}{[\text{Au}]}n \text{ or } \frac{[\text{Au}^-]}{[\text{Au}^-]} = \frac{n}{n_i} \]
  Au acceptor ↑ in “n⁺” Si (100x if \( n_i(1000°C) = 7.14 \times 10^{18} \) - \( 10^{21}\text{cm}^{-3} \) doping level)

- Ion pairing model: \( \text{AuP} \leftrightarrow \text{less strain} \)
  Increases with Phosphorus concentration

- Coulombic attraction \( \text{Au}^+ + \text{P} \rightarrow \text{Au}^-\text{P}^- \)

- Interaction with point defects \( \text{V}^- \uparrow\uparrow \) in “n⁺” \( \text{Au}_i + \text{V}^- \leftrightarrow \text{Au}_s \) at the trapepd site

- Intrinsic gettering - trapping on dislocations and SF which surround precipitates.
  Dislocations have compressive and tensile stress - accommodate smaller and larger atoms
Limits and Future Trends in Technology and Modeling (1)

- Eliminate defects from wafers: particles, contaminants, clean room.
  - SMIF Box (Standard Mechanical Interface): limit clean room size, transport between stations in a clean box

- Wafer cleaning (next slide)

- Gettering:
  - intrinsic (less extrinsic),
  - control $O_i$, $C_s$,
  - use low T processing,
  - use modeling tool $\rightarrow$ point defects engineering,
  - release, diffuse, entrap.
Limits and Future Trends in Technology and Modeling (2)

- Wafer cleaning in future ICs
  - less chemicals (liquids, vapors), more diluted (disposal)
  - New cleaning:
    - Use ozone
    - Dry and vapor phase, (Vapors, Plasmas) environment! Cluster tools
    - Low Energy Physical Processes (sputtering)
    - Photochemically enhanced clean

Watch for surface roughness
Summary of Key Ideas

- A three-tiered approach is used to minimize contamination in wafer processing.
- Particle control, wafer cleaning and gettering are some of the "nuts and bolts" of chip manufacturing.
- The economic success (i.e. chip yields) of companies manufacturing chips today depends on careful attention to these issues.
- Level 1 control - clean factories through air filtration and highly purified chemicals and gases.
- Level 2 control - wafer cleaning using basic chemistry to remove unwanted elements from wafer surfaces.
- Level 3 control - gettering to collect metal atoms in regions of the wafer far away from active devices.
- The bottom line is chip yield. Since "bad" die are manufactured alongside "good" die, increasing yield leads to better profitability in manufacturing chips.