CVD: General considerations.

PVD: Move material from bulk to thin film form.
• Limited primarily to metals or simple materials.
• Limited by thermal stability/vapor pressure considerations.
• Typically requires relatively high temperature and surface experiences high temperature molecules.
• Today used primarily for deposition of Al, Al:Cu, Au.
• Natural coverage: line of sight, with \( \cos \theta \) distribution.

CVD: Provides opportunity to deposit thin films of complex materials and in principle can be accomplished at low or modest substrate temperatures.
• Natural coverage: conformal.
• Used today primarily for dielectrics and refractory conductors.
CVD Process

Continuous gas flow

Diffusion of reactants

Boundary layer

Deposited film

Silicon substrate
Chemical reaction and typical energetics for CVD.

\[ AB + C + (\text{inert carrier}) \rightarrow A + BC + (\text{inert carrier}) \]
Reactions and reaction control in CVD.

Generally energy is needed to stimulate the reaction (overcome activation energy $E_A$) and to control film growth.

Thermal energy.
- CVD: normal chemical vapor deposition.
- LPCVD: low pressure CVD.
- APCVD: Atmospheric pressure CVD.

Plasma.
- PECVD: plasma enhanced CVD.
- HDPCVD: High density plasma enhanced CVD.
- RPECVD: remote plasma enhanced CVD.
- Etc...
Polysilicon CVD

\[ \text{SiH}_4(\text{gas}) + \text{H}_2(\text{gas}) \rightarrow 2\text{H}_2(\text{gas}) + \text{PolySilicon (solid)} \]
Film Formation during Plasma-Based CVD

Same as CVD, but plasma accelerates reactions; charged products deposit anisotropically; and extra energy in products increases the final film quality.
Some exemplary data for deposition of polysilicon:

High temperature: deposition limited by mass transport
Low temperature: deposition limited by chemical reaction

- $\text{SiH}_4$
- $\text{SiH}_2\text{Cl}_2$
- $\text{SiHCl}_3$
- $\text{SiCl}_4$
A different way to plot the growth rate:
CVD Reactor designs – examples.

Horizontal flow reactors, (a) and (b).

Pancake reactor (c), and barrel reactor (d).

Single wafer reactors, (e) and (f).
Plasma Enhanced CVD Processing System

Process chamber

Gas inlet

Capacitive-coupled RF input

Chemical vapor deposition

Wafer

Susceptor

Heat lamps

Exhaust

CVD cluster tool
High Density Plasma Deposition Chamber

- Popular since ~ 1995
- High density plasma
- Highly directional due to wafer bias
- **Fills** high aspect ratio gaps (*deposition mode*)
- Backside He cooling to relieve high thermal load
- Simultaneously deposits and etches film to prevent bread-loaf and key-hole effects

Photograph courtesy of Applied Materials, Ultima HDPCVD Centura
Typical deposition conditions and properties of silicon oxide films deposited using HDP CVD.

<table>
<thead>
<tr>
<th>Process parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source rf power</td>
<td>2000-4000 W</td>
</tr>
<tr>
<td>Gases</td>
<td>SiH₄/Ar/O₂ = 32-45/0-40/43-60 sccm.</td>
</tr>
<tr>
<td>Pressure</td>
<td>&lt;5 mTorr</td>
</tr>
<tr>
<td>Deposition/sputtered ratio</td>
<td>3.2:1 (filled 0.25 μm, 2.5:1 aspect ratio).</td>
</tr>
<tr>
<td>Deposition temperature</td>
<td>250-350°C</td>
</tr>
<tr>
<td>Deposition rate</td>
<td>180-400 nm/min</td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.46 ± 0.003</td>
</tr>
<tr>
<td>Film stress (0.7 μm, 25°C)</td>
<td>(-)1.0-1.6 x 10⁹ dynes/cm².</td>
</tr>
<tr>
<td>Wet-etching (6:1 buffered HF)</td>
<td>1.6-1.8 x that of thermal oxide.</td>
</tr>
</tbody>
</table>
Films of silicate glass deposited on 0.3 micron features.

Conformal coverage of LPCVD process based on TEOS.

“Bread-loaf” profile of PECVD process based on TEOS.

Unique profile of HDP CVD process based on silane.

Polysilicon or polycrystalline silicon deposition.

Uses: primarily as conductive material.
• Conductor in CMOS, bipolar, and related structures.
• Resistors.
• Electrodes for internal capacitors (DRAM for example).

Advantages:
• Compatible with silicon.
• Withstands subsequent high temperature processing.
• Excellent interface with SiO$_2$ (low defect density etc.).
• Conformal coverage.

A layer of polysilicon is then deposited onto the silicon dioxide surface using chemical vapor deposition. This material will serve as the transistor's gate.
Polysilicon silicon deposition

Primary basic chemistry:

\[ \text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2 \]

Very simple chemistry.
Single starting reagent.
Starting material readily available in high purity.
No bothersome products.
No significant side reactions.
Reaction readily takes place at modest temperature.

Pressure \( \sim 0.3-1.0 \) torr.
\( T_{\text{reaction}} \sim 580^\circ - 650^\circ\text{C} \).
Lower temperatures give too slow reaction.
Higher temperatures give rise to gas phase reaction (particulates).
Deposition rate in realm of 0.01 micron/min.
Deposition time approx. 2.5 hours for 0.3 micron film.
Silicon dioxide and related dielectric material deposition

Uses:
- Gate dielectric (MOS, CMOS etc.)
- Isolation of internal transistor from metal conductor.
- Outer metallization insulation.
- Storage of charge – capacitance (EPROM).
- Passivation layers.
- Dopant Diffusion sources.
- Diffusion and implantation masks.

Structure generally amorphous with SiO$_2$ in local tetrahedral configuration.

Sometimes referred to as USG for undoped silicate glass.
Silicon dioxide deposition.

Basic chemistry: low temperature silane process.

$$\text{SiH}_4 + \text{O}_2 \text{ (nitrogen carrier)} \rightarrow \text{SiO}_2 + 2\text{H}_2$$

Pressure $\sim <1$ atmosphere; silane partial pressure in realm of 1 torr; oxygen in excess.

$T_{\text{reaction}} \sim 310^\circ - 450^\circ\text{C}.$

Activation energy approx. 0.4 eV.

Films slightly porous, densification at 700$^\circ$-1000$^\circ$C necessary for high quality films.

Film quality measurements:

<table>
<thead>
<tr>
<th>Property</th>
<th>Low T silane</th>
<th>Thermal oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant</td>
<td>3.2-3.4</td>
<td>3.9</td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.44</td>
<td>1.46</td>
</tr>
<tr>
<td>Etch rate*</td>
<td>3 - &gt;10</td>
<td>(1.0)</td>
</tr>
</tbody>
</table>

Slightly Porous
**Silicon dioxide deposition**

Basic chemistry: low temperature plasma enhanced process.

\[
\text{SiH}_4 + 2\text{N}_2\text{O (argon carrier)} \rightarrow \text{SiO}_2 + 2\text{H}_2 + 2\text{N}_2
\]

Pressure \(~\) .

\(T_{\text{reaction}} \sim 200^\circ - 400^\circ\text{C}.

Activation energy approx. 0.4 eV.

Films slightly porous, densification at 700\(^\circ\)-1000\(^\circ\)C necessary for high quality films.

<table>
<thead>
<tr>
<th>Property</th>
<th>Low T PECVD</th>
<th>Thermal oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant</td>
<td>4-5</td>
<td>3.9</td>
</tr>
<tr>
<td>Refractive index</td>
<td>(~1.46)</td>
<td>1.46</td>
</tr>
<tr>
<td>Etch rate*</td>
<td>(~2-10)</td>
<td>(1.0)</td>
</tr>
<tr>
<td>Dielectric strength</td>
<td>4-8 MV/cm</td>
<td>12-15 MV/cm</td>
</tr>
</tbody>
</table>

Slightly Silicon Rich
**Silicon dioxide deposition**

Basic chemistry: TEOS (tetraethyl orthosilicate) process.

\[
\text{Si(OCH}_2\text{CH}_3)_4 \text{ (nitrogen carrier)} \rightarrow \text{SiO}_2 + 4\text{C}_2\text{H}_4 + 2\text{H}_2\text{O}
\]

*TEOS is stored as liquid (but used as gas phase reactant).*

Conventional CVD (medium temperature) process.
- Impurities present such as C – add O\(_2\) to minimize.
- \(T_{\text{reaction}}\) 680-730\(^\circ\)C (cannot be used over Al).
- 0.03 micron/minute deposition rate.
- Improved step coverage relative to silane process.

PE CVD (low temperature) process.
- \(T_{\text{reaction}}\) 250-425\(^\circ\)C.
- Total pressure 2-10 torr.
- 0.1 micron/minute deposition rate.
CVD Silicon Nitride Deposition.

Uses:
- Final passivation and mechanical protection.
- Mask for selective oxidation of Si.
- Charge storage dielectric in MOS capacitors.
- Sidewall structures in MOSFETs.
- CMP stop-layer.

Basic chemistry: low pressure CVD process.

$$3\text{SiCl}_2\text{H}_2 + 4\text{NH}_3 \text{ (carrier)} \rightarrow \text{Si}_3\text{N}_4 + 6\text{H}_2 + 6\text{HCl}$$

\[ T_{\text{reaction}} \sim 700^\circ - 800^\circ \text{C.} \]

Deposition rate 0.01 micron/min.

Basic chemistry: Plasma enhanced CVD process.

$$\text{SiH}_4 + \text{NH}_3 \rightarrow \text{Si}_x\text{N}_y\text{H}_z + \text{H}_2$$

\[ T_{\text{reaction}} \sim 200^\circ - 400^\circ \text{C.} \]

$P=0.2-0.3$ torr

Deposition rate 0.05 micron/min.
Other useful CVD deposition processes:

**WSi₂: Tungsten Silicide.**

*Uses:*
- Local interconnect (bit lines in memory devices).
- Adhesion layers (for W for example).

\[
WF_6 + 2 \text{SiH}_4 \rightarrow WSi_2 + 6 \text{HF} + H_2 \quad (300-400^\circ\text{C, low pressure})
\]

\[
2WF_6 + 7 \text{SiH}_2\text{Cl}_2 \rightarrow 2WSi_2 + 3\text{SiCl}_4 + 12\text{HF} + 2\text{HCl} \quad (600^\circ\text{C})
\]

**TiN: Titanium nitride.**

*Uses:*
- Diffusion barriers (for Cu for example).
- Adhesion layers.

\[
6 \text{TiCl}_4 + 8 \text{NH}_3 \rightarrow 6 \text{TiN} + 24 \text{HCl} + \text{N}_2 \quad (600^\circ\text{C, low pressure})
\]
CVD W (tungsten) Deposition

Uses:
  Metal vias (“plug”).
  Local metallization.

Basic chemistries:

\[
2 \text{WF}_6 + 3 \text{Si} \rightarrow 2 \text{W} + 3 \text{SiF}_4 \quad \text{(300}^\circ\text{C, 0.015 micron)}
\]
\[
\text{WF}_6 + 3 \text{H}_2 \rightarrow \text{W} + 6 \text{HF} \quad \text{(low pressure, 450}^\circ\text{C)}
\]
\[
2 \text{WF}_6 + 3 \text{SiH}_4 \rightarrow 2 \text{W} + 3 \text{SiF}_4 + 6 \text{H}_2 \quad \text{(low pressure, 300}^\circ\text{C)}
\]
<table>
<thead>
<tr>
<th>Product</th>
<th>Reactants</th>
<th>Method</th>
<th>Temperature (°C)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-silicon</td>
<td>SiH₄</td>
<td>LPCVD</td>
<td>580 – 650</td>
<td>May be in situ doped</td>
</tr>
<tr>
<td>Silicon Nitride</td>
<td>SiH₄ + NH₃</td>
<td>LPCVD</td>
<td>700 – 900</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SiCl₂H₂ + NH₃</td>
<td>LPCVD</td>
<td>650 – 750</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SiH₄ + NH₃</td>
<td>PECVD</td>
<td>200 – 350</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SiH₄ + N</td>
<td>PECVD</td>
<td>200 – 350</td>
<td></td>
</tr>
<tr>
<td>SiO₂</td>
<td>SiH₄ + O₂</td>
<td>APCVD</td>
<td>300 – 500</td>
<td>Poor step coverage</td>
</tr>
<tr>
<td></td>
<td>SiH₄ + O₂</td>
<td>PECVD</td>
<td>200 – 350</td>
<td>Good step coverage</td>
</tr>
<tr>
<td></td>
<td>SiH₄ + N₂O</td>
<td>PECVD</td>
<td>200 – 350</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Si(OC₂H₅)₄ [TEOS]</td>
<td>LPCVD</td>
<td>650 – 750</td>
<td>Liquid source, conformal</td>
</tr>
<tr>
<td></td>
<td>SiCl₂H₂ + N₂O</td>
<td>LPCVD</td>
<td>850 – 900</td>
<td>conformal</td>
</tr>
<tr>
<td>Doped SiO₂</td>
<td>SiH₄ + O₂ + PH₃</td>
<td>APCVD</td>
<td>300 – 500</td>
<td>PSG</td>
</tr>
<tr>
<td></td>
<td>SiH₄ + O₂ + PH₃</td>
<td>PECVD</td>
<td>300 – 500</td>
<td>PGS</td>
</tr>
<tr>
<td></td>
<td>SiH₄ + O₂ + PH₃ + B₂H₆</td>
<td>APCVD</td>
<td>300 – 500</td>
<td>BPSG, low temperature flow</td>
</tr>
<tr>
<td></td>
<td>SiH₄ + O₂ + PH₃ + B₂H₆</td>
<td>PECVD</td>
<td>300 – 500</td>
<td>BPSG, low temperature flow</td>
</tr>
</tbody>
</table>