THERMAL OXIDATION

- SiO$_2$ and the Si/SiO$_2$ interface are the principal reasons for silicon's dominance in the IC industry.

SiO$_2$:
- Easily selectively etched using lithography.
- Masks most common impurities (B, P, As, Sb).
- Excellent insulator ($\rho > 10^{16} \ \Omega \text{cm}$, $E_g > 9 \ \text{eV}$).
- High breakdown field ($10^7 \ \text{Vcm}^{-1}$).
- Excellent junction passivation.
- Stable bulk electrical properties.
- Stable and reproducible interface with Si.

- No other known semiconductor/insulator combination has properties that approach the Si/SiO$_2$ interface.
### SIA NTRS Roadmap

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node (half pitch)</td>
<td>250 nm</td>
<td>180 nm</td>
<td>130 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
<td>18 nm</td>
</tr>
<tr>
<td>MPU Printed Gate Length</td>
<td>100 nm</td>
<td>70 nm</td>
<td>53 nm</td>
<td>35 nm</td>
<td>25 nm</td>
<td>18 nm</td>
<td>13 nm</td>
<td>10 nm</td>
<td></td>
</tr>
<tr>
<td>DRAM Bits/Chip (Sampling)</td>
<td>256M</td>
<td>512M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>32G</td>
<td>64G</td>
<td>128G</td>
<td>128G</td>
</tr>
<tr>
<td>MPU Transistors/Chip (x10^9)</td>
<td>550</td>
<td>1100</td>
<td>2200</td>
<td>4400</td>
<td>8800</td>
<td></td>
<td></td>
<td>14,000</td>
<td></td>
</tr>
<tr>
<td>Gate Oxide Thickness Equivalent (nm)</td>
<td>1.2</td>
<td>0.9</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Operating Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Dielectric Leakage (mA/µm @ 100°C) MPU</td>
<td>170</td>
<td>230</td>
<td>330</td>
<td>1000</td>
<td>1670</td>
<td>1670</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thickness Control (% 3σ)</td>
<td>&lt; ±4</td>
<td>&lt; ±4</td>
<td>&lt; ±4</td>
<td>&lt; ±4</td>
<td>&lt; ±4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min Supply Voltage (volts)</td>
<td>1.8-2.5</td>
<td>1.5-1.8</td>
<td>1.2-1.5</td>
<td>0.9-1.2</td>
<td>0.8-1.1</td>
<td>0.7-1.0</td>
<td>0.6-0.9</td>
<td>0.5-0.8</td>
<td>0.5-0.7</td>
</tr>
</tbody>
</table>

- **SiO₂** is not the gate dielectric of the future
- High-K dielectrics are now being used to reduce leakage

\[
C = \frac{K \cdot \varepsilon \cdot A}{d}
\]
Si and SiO$_2$

- Oxidation occurs at the Si/SiO$_2$ interface
- A pure Si layer will oxidize at room temperature
  - Rapid growth to 0.5 to 1 nm (5-10 Angstroms)
  - Final growth of 1-2 nm
- Oxidation involves a volume expansion
  - SiO$_2$ is 30% larger than Si
  - Volume expansion $1.3^3 \sim 2.2$
- Induces stress where confined, especially in 2D and 3D structures, stress effects play a dominant role.
Basic Concept

- $O_2$ or $H_2O$ diffuse to Si interface
- Oxidation reaction consumes silicon moving the interface down and the $SiO_2$ up as material is consumed and the volume increases

$SiO_2$ volume expansion can cause stress on the surface
- 30% expansion in all directions when unconstrained
- Stress induced when volume constrained
SEM of LOCOS

Volume Expansion

Bird’s Beak Topology lateral growth

Deposited Polysilicon

Location of Si$_3$N$_4$ Mask

Original Si Surface

Volume Expansion

SiO$_2$

Si Substrate

Stress at the Si/Si$_3$N$_4$ interface
Structure of Silica Glass

- SiO₂ is amorphous even though it grows on a crystalline substrate (Figure 3-15)
  - Based on SiO₄ tetrahedra shown above.
  - Bridging oxygen atoms share to form crystal like quartz
  - Time to form appropriate rotational forms for full crystallization not available; therefore, forms rarely observed in IC
  - Lattice doesn’t match Si, but there is a short range order

Image credit: Prentice Hall
Si/SiO₂ Stresses

• Compressive stress due to constrained growth region
  – Grow upward
  – Stress as large as $5 \times 10^9$ dyne cm$^{-2}$
• At high temperature, viscous flow may reduce stress

• There is a large difference in the thermal expansion coefficients
  – Stress as large as $1-2 \times 10^8$ dyne cm$^{-2}$

• Wafer curvature can be produced from unbalanced stress between the top and bottom of a wafer
  – Selective etching of one surface will produce curvature
Oxide Layer: Intel 90 nm Process

- SiO$_2$ is amorphous even though it grows on a crystalline substrate
  - Lattice doesn’t match Si
  - There is a short range order

- Intel SiO$_2$ of approx. 3-5 atomic layers

- Deal and Grove (1965) showed that SiO$_2$ growth follows a linear parabolic law.
  - Where model inadequate: thin oxides, oxides grown in mixed ambient, oxides grown on 2D and 3D Si surfaces, oxides grown on heavily doped substrates
Oxide Growth Charges

- Four charges are associated with insulators and insulator/semiconductor interfaces.
  - $Q_f$ - fixed oxide charge
  - $Q_{ht}$ - interface trapped charge
  - $Q_m$ - mobile oxide charge
  - $Q_{ot}$ - oxide trapped charge

- Deal defined nomenclature in 1980 for electrical charge defects

- Processing to reduce charges:
  - High temperature inert anneals in Ar or $N_2$ toward the end of process flow.
  - Moderate temperature anneal ($400 \, ^\circ C$) in $H_2$ or forming gas ($N_2/H_2$)
Wafer Fabrication Equipment

- Oxidation systems are conceptually very simple.
  - Dry or wet, 600 – 1200 °C
- In practice today, vertical furnaces, RTO systems and fast ramp furnaces all find use.

- Thermal oxidation can potentially be used in many places in chip fabrication. In practice, deposited SiO₂ layers are increasingly being used (lower Dt).
Conventional Oxidation System

Wafer loading should use cantilever or elevators (perpendicular) to avoid touching the walls.

Vertical furnaces are also used. Better uniformity, easier automation, cleaner - no contact with the tub.

Dry or wet oxidation

Ramping of T from/to 800 °C (10 °C/sec)

Add HCl or TCA for gettering purpose (metals, Na⁺)

Figure 6-7 Conceptual silicon oxidation system.

At 1000 °C, in wet O₂ is approx. 0.1 nm per second. It approx. doubles for every 100 °C rise.
Rapid Thermal Oxidation

- [http://www.iue.tuwien.ac.at/phd/hollauer/node13.html](http://www.iue.tuwien.ac.at/phd/hollauer/node13.html)

- Reduced time for temperature ramp
  - 100 °C per second vs. <10 °C per second

- Reduced size chamber for smaller number of wafers
  - Single wafer vs. multiple boats of 10-50 wafers

- Simple temperature feedback
  - Pyrometer monitors wafer vs. multiple zones with thermocouple that are preset at installation (need +/- 0.5 °C control)
Measurement Methods

- Physical
- Optical
- Electrical Devices (MOS Capacitor gate)
Physical Step Height Measurement

- By etching away part of the SiO$_2$, the resulting step height between the original Si and new SiO$_2$ height can be made.

- Atomic Force Microscope
  - Technique to visual Figure 1-3

- Cross section wafer and use an SEM
  - As in Figure 6-4 or a TEM in Figure 3-15
Optical Measurement

- Optical (usually non-destructive): thick oxides (color chart, ellipsometry, reflectance)
  but for thin oxides: ellipsometry

**REFLECTANCE**

white or monochromatic light

For monochromatic light minima and maxima in the reflected beam allows to determine $x_{ox}$ (fringes, spectrometers with sweeping wavelength $\lambda$ for fixed $\phi$ we can find extrema).

[Good for a few tens of nm]

Ellipsometry uses polarized light and detect the change in polarization of the reflected light due to a film (thickness, index of refraction)

\[
\begin{align*}
\lambda &= \frac{2 \cdot n_1 \cdot x_0 \cdot \cos(\beta)}{m} \\
\text{maxima at } m &= 1, 2, 3, \ldots \\
\text{minima at } m &= \frac{1}{2}, \frac{3}{2}, \frac{5}{2}, \ldots \\
\beta &= \arcsin \left( \frac{n_2 \cdot \sin(\phi)}{n_1} \right)
\end{align*}
\]

Color chart ($x_{ox} > 50\text{nm}$) \(\rightarrow\) not destructive interference will affect the reflected light \(\rightarrow\) color correlated with thickness of a dielectric layer (10-20 nm accuracy)
Optical Methods

- Optical color pattern
  - [http://cleanroom.byu.edu/color_chart.phtml](http://cleanroom.byu.edu/color_chart.phtml)
  - Color Chart description in Table A.7 on p. 790
Electrical Measurements

- Direct electrical measurement of device type parameters
- Oxides are typically used as the dielectric layer in a capacitor
  - Doped silicon conductor, SiO$_2$ dielectric, doped polysilicon or metal conductor layers similar to an MOS transistor.

- Typically Capacitance-Voltage or C-V measurements are taken
  - A DC bias with an AC voltage source to measure changes in impedance with frequency
  - Widely used for MOS devices, gate oxide parameters, and carrier lifetimes
C-V Measurements

- DC bias + small AC high frequency signal applied.

\[ C = \frac{dQ}{dV} \]

Charge Density

\[ |Q_G| = |Q_D| = N_D x_D \]

\[ |Q_G| = N_D x_D + Q_I \]

a) Accumulation majority carrier drawn to surface

\[ C_{ac} = \frac{\varepsilon_{ac} \cdot A}{x_{ac}} \]

b) Depletion minority carrier drawn to surface majority carriers repelled

\[ C_D = \frac{\varepsilon_{si} \cdot A}{x_D} \]

c) Inversion minority carrier layer exists

---

SILICON VLSI TECHNOLOGY
Fundamentals, Practice and Modeling
By Plummer, Deal & Griffin

© 2000 by Prentice Hall
Upper Saddle River NJ
C-V Plot

- LF curve - inversion layer carriers can be created and recombine at AC signal frequency so $C_{inv}$ is just $C_{ox}$.
- HF curve (100 kHz to 1 MHz) - inversion layer carriers cannot be generated fast enough to follow the AC signal so $C_{inv}$ is $C_{ox} + C_D$.
- Deep depletion - "DC" voltage is applied fast enough that inversion layer carriers cannot follow it, so $C_D$ must expand to balance the charge on the gate.
- C-V measurements can be used to extract quantitative values for:
  - $t_{ox}$ - oxide thickness
  - $N_A$ - the substrate doping profile
  - $Q_f$, $Q_{it}, Q_{m}, Q_{opt}$ - oxide, interface charges
MOS C-V Band Diagram

Figure 6-10 Band diagram for the MOS capacitor in (a) accumulation, (b) depletion, and (c) inversion.

To avoid deep depletion:

\[ U = \frac{N_i}{\tau_0} \]

\[ J_{gen} = \frac{q\mu W}{\tau_0} \]

\[ \frac{dV}{dt} \leq \frac{J_{gen}}{C} = \frac{q\mu W}{\tau_0 C_{ox}} = 0 \text{ V/sec} \]

\[ \Delta Q_G = \Delta Q_D \]

\[ X_D = X_{D_{max}} \rightarrow C_D = C_{D_{max}} \]

Holes generated in the depletion layer and attracted by the gate source the DL when [V_G] increases.

High frequency AC signal changes faster than Q_L can respond (generation is slow).

SILICON VLSI TECHNOLOGY
Fundamentals, Practice and Modeling
By Plummer, Deal & Griffin

© 2000 by Prentice Hall
Upper Saddle River NJ
Charges Derived

$Q_{in}, Q_{sh}$ have similar effect as $Q_t$ (shift characteristics)

Due to traps

Traps cannot charge or discharge - do not respond to HF signal

Figure 6-13 BF MOS CV curves illustrating some of the nonidealities that can be present in actual experimental structures. A, B, and C illustrate the effects of interface states with different energy levels in the silicon bandgap.

$Q_t$ respond to DC voltage → stretch out → change in $E_F (V_C)$, charges at $E_R$.

Stress of the oxide (ex. charge injection, radiation) → C-V degradation (→ time to breakdown, charge to breakdown)

Figure 6-14 Typical experimental HF and LF CV curves used to extract the interface state density $D_0$ as a function of energy in the bandgap. The $D_0$ plot is typical of extracted data.
Models and Simulation

- Deal-Grove Model Plots

Oxidation rate for (100) silicon in dry O₂.  
Oxidation rate for (100) silicon in wet O₂.
Deal Grove Model

- The basic model for oxidation was developed in 1965 by Deal and Grove.
  - A linear parabolic model

\[
\begin{align*}
\text{Si} + \text{O}_2 & \rightarrow \text{SiO}_2 \quad (2) \\
\text{Si} + 2\text{H}_2\text{O} & \rightarrow \text{SiO}_2 + 2\text{H}_2 \quad (3)
\end{align*}
\]

F1: Transport of Oxygen to oxide surface
   Gas phase diffusion through stagnant boundary layer
   Equilibrium concentration in a solid (based on partial pressures)

F2: Diffusion of oxidant through the oxide

F3: Reaction with the Silicon surface

In steady-state, \( F_1 = F_2 = F_3 \) where flux is in molecules cm\(^{-2}\) sec\(^{-1}\)
Deal Grove Model

Transport of Oxygen to oxide surface

\[ F_i = h_i (C_o - C_s) \]

Mass transport coefficient

Surface – Henry’s Law

\[ C_o = \frac{H \cdot P_o}{C^*} \]

\[ C^* = H \cdot P_o \approx C_o \]

\[ P_o = \frac{h_i}{H \cdot kT} \]

Ideal Gas Law

Reaction with the Silicon surface

Interface reaction rate

\[ F_i = k_s C_j \]

Diffusion of oxidant through the oxide

Fick’s Law - Diffusivity

\[ F_2 = -D \frac{\partial C}{\partial x} = D \left( \frac{C_o - C_i}{x_o} \right) \]

The gradient is approx. a constant
Deal-Grove Model (2)

- Under steady state conditions, \( F_1 = F_2 = F_3 \) so

\[
F_1 = h \cdot (C^* - C_0)
\]

\[
F_2 = D \left( \frac{C_o - C_i}{x_o} \right)
\]

\[
F_3 = k_s C_i
\]

\[
C_i = \frac{C^*}{1 + \frac{k_s x_o}{D}} \approx \frac{C^*}{1 + \frac{k_s x_o}{D}}
\]

\[
C_o = \frac{C^*}{1 + \frac{k_s x_o}{h D}} \approx C^*
\]

h very large and can be neglected

- Note that the simplifications are made by neglecting \( 1/h \) where \( h \) large. This results in a very good approximation.

- Combining the above, we have

\[
\frac{dx}{dt} = \frac{F}{N_i}
\]

\[
F_i = k_s C_i
\]

\[
\frac{dx}{dt} = \frac{F}{N_i} = \frac{k_s C^*}{N_i \left(1 + \frac{k_s x_o}{h D} \right)}
\]

Oxygen molecules incorporated per unit volume of oxide grown
Deal-Grove Model (3)

\[
\frac{dx}{dt} = \frac{E}{N_i} = \frac{k_s C^*}{N_i \left(1 + \frac{k_s}{h} + \frac{k_s x_2}{D}\right)}
\]

\[
N_i \int_{x_i}^{x_f} \left(1 + \frac{k_s}{h} + \frac{k_s x_2}{D}\right) \cdot dx = k_s C^* \cdot \int_0^t dt
\]

\[
\frac{x_i^2 - x_f^2}{B} + \frac{x_0 - x}{B/A} = t
\]

where \( B = \frac{2DC^*}{N_i} \) (parabolic rate constant, \( F_2 \) dominant)

and \( \frac{B}{A} = \frac{C^*}{N_i \left(1 + \frac{1}{k_s} + \frac{1}{h}\right)} \) (linear rate constant, \( F_3 \) dominant)

Defining initial conditions of the interface:

\[
\tau = \frac{x_i^2}{B} + \frac{x_0}{B/A}
\]

\[
\frac{x_i^2}{B} + \frac{x_0}{B/A} = t + \tau
\]
Deal-Grove Model (4)

- Solving for oxide thickness as a function of time.

\[
\frac{x_0^2}{B} + x_0\frac{B}{A} = t + \tau
\]

\[
x_0^2 + A\cdot x_0 - B\cdot (t + \tau) = 0
\]

\[
x_0(t) = \frac{A}{2} \left[ \sqrt{1 + \frac{t + \tau}{A^2 / 4B}} - 1 \right]
\]

For thin oxide, \(x\) small

\[
\frac{x_0^2}{B} + x_0\frac{B}{A} \Rightarrow \frac{x_0}{B / A} = t + \tau
\]

\[
x_0 = \frac{A}{B} (t + \tau)
\]

For thick oxide, \(x\) large

\[
\frac{x_0^2}{B} + x_0\frac{B}{A} \Rightarrow \frac{x_0^2}{B} = t + \tau
\]

\[
x_0^2 = B\cdot (t + \tau)
\]
Deal-Grove Model (5)

\[ x_0 = \frac{A}{2} \left\{ 1 + \frac{1 + t + \tau}{A^2/4B} - 1 \right\} \]
\[ \tau = \frac{x_i^2}{B} + \frac{x_o^2}{B/A} \]

\[ B = \frac{2DC^s}{N_1} \quad \text{F}_2 \text{ dominant} \]

\[ \frac{B}{A} = \frac{C^s}{N_1} \left( \frac{1}{k_S} + \frac{1}{h} \right) \leq \frac{C^s k_S}{N_1} \quad \text{F}_2 \text{ dominant} \]

\[ C_1 \approx 0 \]

Fast reaction - diffusion limits oxidation (thick oxides)

\[ k_s x_0 / D \ll 1 \]
\[ C_1 \approx C^* \]

Diffusion fast compared to chemical reaction for thin oxides.

\[ x_o = \frac{A}{B} \cdot (t + \tau) \]

For about 50-200 nm, \( k_s, D(T) \)

\[ x_o^2 = B \cdot (t + \tau) \]
• The rate constants B and B/A have physical meaning (oxidant diffusion and interface reaction rate respectively).

<table>
<thead>
<tr>
<th>Ambient</th>
<th>B</th>
<th>B/A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry O₂</td>
<td>$C_1 = 7.72 \times 10^5 \text{ m}^3 \text{ hr}^{-1}$</td>
<td>$C_2 = 6.23 \times 10^6 \text{ m}^3 \text{ hr}^{-1}$</td>
</tr>
<tr>
<td>Wet O₂</td>
<td>$C_1 = 2.14 \times 10^5 \text{ m}^3 \text{ hr}^{-1}$</td>
<td>$C_2 = 9.95 \times 10^6 \text{ m}^3 \text{ hr}^{-1}$</td>
</tr>
<tr>
<td>H₂O</td>
<td>$C_1 = 3.86 \times 10^5 \text{ m}^3 \text{ hr}^{-1}$</td>
<td>$C_2 = 1.63 \times 10^6 \text{ m}^3 \text{ hr}^{-1}$</td>
</tr>
</tbody>
</table>

\[
B = C_1 \exp\left(-\frac{E_1}{kT}\right)
\]

\[
\frac{B}{A} = C_2 \exp\left(-\frac{E_2}{kT}\right)
\]

• Numbers are for (111) silicon, for (100) divide $C_2$ by 1.68.

• Plots of B, B/A using the values in the above Table.
Deal-Grove Model

Oxidation rate for (100) silicon in dry $O_2$. Oxidation rate for (100) silicon in wet $O_2$.

- Wet $O_2$ rate is significantly higher than dry $O_2$. The oxidant solubility is higher.
- Dry $O_2$ used for thin oxides and controlled depths, wet $O_2$ for thicker films.
Example Problem 6.13

Calculated (100) silicon dry O₂ oxidation rates using Deal Grove.

Example: Problem 6.13 in the text:
- a) 3 hrs in O₂ @ 1100 °C = 0.21 μm
- b) 2 hrs in H₂O @ 900 °C = 0.4 μm
- c) 2 hrs in O₂ @ 1200 °C = 0.5 μm total oxide thickness.

Calculated (100) silicon H₂O oxidation rates using Deal Grove.
Volume Mismatch in Si/SiO₂ System; Recessed LOCOS

Example: \( \text{H}_2\text{O@1000°C}; \) Find time to get planar surface?

2.2X volume expansion \( \Rightarrow \)

45% \( y_{\text{ox}} = y_{\text{Si}} \) so \( y_{\text{ox}} = y_{\text{Si}}/0.45 \)

Total oxide thickness to be grown:

\( y_{\text{ox}} = y_{\text{Si}}/0.45 = y_{\text{Si}} + 0.5\mu\text{m} \)

\( y_{\text{Si}} = 0.41\mu\text{m} \)

\( y_{\text{ox}} = 0.91\mu\text{m} \)

\[ B = 3.86 \times 10^2 \exp \left( -\frac{0.78 \text{ eV}}{kT} \right) = 0.316 \mu\text{m}^2\text{hr}^{-1} \]

\[ \frac{B}{A} = 1.63 \times 10^6 \exp \left( -\frac{2.05 \text{ eV}}{kT} \right) = 0.75 \mu\text{m} \text{ hr}^{-1} \]

\[ t = \frac{x_0^2}{B} + \frac{x_0}{B/A} = \frac{(0.91)^2}{0.316} + \frac{0.91}{0.75} \approx 3.83 \text{ hrs} \]

For \( \text{H}_2\text{O} \)

Time for dry oxidation would be unrealistically long.
Thin Oxide Growth Models

- A major problem with the Deal Grove model was recognized when it was first proposed - it does not correctly model thin $O_2$ growth kinetics.
-Experimentally $O_2$ oxides grow much faster for $\approx 20$ nm than Deal Grove predicts.

- MANY models have been suggested in the literature.

1. Reisman et. al. Model

$$x_O = a(t + t_i)^b \quad \text{or} \quad x_O = a\left(t + \left(\frac{x_i}{a}\right)^b\right)$$

- Power law “fits the data” for all oxide thicknesses.
  - $a$ and $b$ are experimentally extracted parameters.
- Physically - interface reaction controlled, volume expansion and viscous flow of $SiO_2$ control growth.
Thin Oxide Growth Models

2. Han and Helms Model

\[
\frac{dx_O}{dt} = \frac{B_1}{2x_O + A_1} + \frac{B_2}{2x_O + A_2}
\]

- Second parallel reaction added - “fits the data” for all oxide thicknesses.
- Three parameters (one of the A values is 0).
- Second process may be outdiffusion of O\textsuperscript{+} and reaction at the gas/SiO\textsubscript{2} interface.

3. Massoud et. al. Model

\[
\frac{dx_O}{dt} = \frac{B}{2x_O + A} + C \exp\left(-\frac{x_O}{L}\right)
\]

- Second term added to Deal Grove model - higher dx/dt during initial growth.
- \( L \approx 7 \) nm, second term disappears for thicker oxides.
- Easy to implement along with the DG model, used in process simulators.
- Data agrees with the Reisman, Han and Massoud models. (800°C dry O\textsubscript{2} model comparison below.)
Thin Oxide Growth Models

**Figure 6-23** Comparison of three oxidation models for 1 atmosphere dry O₂ oxidation at 800°C.

**Figure 6-24** Comparison of three oxidation models for 1 atmosphere dry O₂ oxidation at 1000°C. The dashed lines are theDeal Grove model.
Additional Growth Considerations

• Dependence on Pressure
  – If Henry’s Law holds, the growth coefficients are dependent on the oxidant just inside the oxide at the gas/SiO₂ interface.
  – This is dependent upon gas pressure
Additional Growth Considerations

- Dependence on Crystal Orientation
  - Oxidation rates are faster on (111) silicon as compared to (100) silicon.
  - Many current structures uses trench etching and growth.
  - The effect may be due to differences in the number of available bonds at the surface.

![Figure 6-27](image_url) Example of an oxidation simulation involving orientation effects using the ATHENA simulator [6.12]. The top and bottom surfaces of the etched trench are (100) surfaces. The trench sidewall is a (110) surface. The oxidation was 30 min at 900°C in H₂O.
2D SiO2 Growth Kinetics

- These effects were investigated in detail experimentally by Kao et. al. about 15 years ago.
- Typical experimental results below.

(Kao et.al)
2D SiO$_2$ Growth Kinetics

Difference in volume $\rightarrow$ problems when expansion is restricted (SiO$_2$ confined)

*Experiments by Kao et al.*:

- Retardation at sharp corners (2X for 500 nm SiO$_2$)
- Retardation larger at low $T$ (no effect at 1200 $^\circ$C)
- Interior (concave) corners oxidize slower than exterior (convex) but both slower than flat Si

*Reasons*:

- Crystal orientation
- Diffusion of oxidant through amorphous SiO$_2$ is the same $\rightarrow$ no dependence on direction
- Stress (volume difference): SiO$_2$ under large compressive stress $\rightarrow$ affect both oxidant transport and reaction at the Si surface

---

*SILICON Fundamentals, Practice and Modeling*
*By Plummer, Deal & Griffin*

© 2000 by Prentice Hall
Upper Saddle River NJ

---

20170329 Page 41
Stress Effects

- Several physical mechanisms seem to be important:
  - Crystal orientation
  - 2D oxidant diffusion
  - Stress due to volume expansion
- To model the stress effects, Kao et. al. suggested modifying the Deal Grove parameters.

\[
k_s'(stress) = k_s \exp(-\frac{\sigma_n V_R}{kT}) \exp(-\frac{\sigma_t V_T}{kT})
\]

\[
D(stress) = D \exp(-\frac{(P)(V_D)}{kT})
\]

\[
C^*(stress) = C^* \exp(-\frac{(P)(V_S)}{kT})
\]

where \(\sigma_n\) and \(\sigma_t\) are the normal and tangential stresses at the interface. \(V_R\), \(V_T\) and \(V_S\) are reaction volumes and are fitting parameters.
Simulating Stress

- In addition, the flow properties of the SiO$_2$ need to be described by a stress dependent viscosity

\[
\eta(\text{stress}) = \eta(T) \frac{\sigma_s V_C / 2kT}{\sinh(\sigma_s V_C / 2kT)}
\]

where $\sigma_s$ is the shear stress in the oxide and $V_C$ is again a fitting parameter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_R$</td>
<td>0.0125 nm$^3$</td>
</tr>
<tr>
<td>$V_D$</td>
<td>0.0065 nm$^3$</td>
</tr>
<tr>
<td>$V_{Si, V_T}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_C$</td>
<td>0.3 nm$^3$ @ 850°C</td>
</tr>
<tr>
<td></td>
<td>0.72 nm$^3$ @ 1050°C</td>
</tr>
<tr>
<td>$\eta(T) - SiO_2$</td>
<td>3.13 x 10$^{10}$ exp(2.19 eV/kT) poise</td>
</tr>
<tr>
<td>$\eta(T) - Si_3N_4$</td>
<td>4.77 x 10$^{10}$ exp(1.12 eV/kT) poise</td>
</tr>
</tbody>
</table>

- These models have been implemented in modern process simulators and allow them to predict shapes and stress levels for VLSI structures (above right).

- ATHENA simulation: Left - no stress dependent parameters, Right – including stress dependence.
Point Defect Based Models

- The oxidation models we have considered to this point are macroscopic models (diffusion coefficients, chemical reactions etc.).

- There is also an atomistic picture of oxidation that has emerged in recent years.
- Most of these ideas are driven by the volume expansion occurring during oxidation and the need for “free volume”.

- In Chapter 3 we described internal oxidation in the following way when discussing SiO$_2$ precipitates as gettering sites (p.141-2):

  \[(1 + 2\gamma)\text{Si}_0 + 2\text{O}_i + 2\beta V \leftrightarrow \text{SiO}_2 + 2\gamma + \text{stress}\]

- Surface oxidation can be thought of in the same way.
  - Vacancies drawn to the surface, interstitials created and move into the bulk silicon (causing other effects?! OED and ORD)
Oxidation Enhanced/Retarded Diffusion

- The connection between oxidation and other processes can then be modeled as shown below.

- Oxidation injects interstitials to create "free volume" for the oxidation process. Oxidation can also consume vacancies for the same reason.
  - These processes increase I concentrations and decrease V concentrations in nearby silicon regions.
  - Any process (diffusion etc) which occurs via I and V will be affected.
Substrate Doping Effects

Concentration Enhanced Oxidation (CEO)

CEO stronger for $N^+$ than $P^+$ ($B/A$ grows, $B$ does not)

CEO for Boron changes $B$ but not $B/A$ due to incorporation in the oxide

N_{Dopant} \ P \rightarrow \mbox{oxide growth by } \uparrow \mbox{ B/A not by B; especially } @ \mbox{ low T about } 3-4X \uparrow \mbox{ due to } \uparrow \mbox{ concentrations}

Properties of oxide do not change for P but change for B

Oxidation needs V for volume expansion so for $\uparrow$ dopant concentrations, charged V $\uparrow$ ($V^+$, $V^+ \rightarrow N^+$-type; $V^+ \rightarrow P^+$-type) $\rightarrow \uparrow \mbox{ B/A}$

Dopant segregation $N^+ \rightarrow \mbox{ Si}$

$P^+ \rightarrow \mbox{ SiO}_2$

Interface changes during oxidation $\rightarrow \mbox{ growth rate changes}$
Complete Process Simulation of Oxidation

- Many of these models (and others in Chapter 6), have been implemented in programs like SUPREM

- Simulation of an advanced isolation structure (the SWAMI process originally developed by Hewlett-Packard), using SSUPREM IV.

- The structure prior to oxidation is on the top left. A 450 min $\text{H}_2\text{O}$ oxidation at 1000 °C is then performed which results in the structure on the top right. An experimental structure fabricated with a similar process flow is shown on the bottom right.

- The stress levels in the growing $\text{SiO}_2$ are shown at the end of the oxidation on the bottom left.
Recessed LOCOS – ATHENA Simulation

Figure 6.41 Simulation of a recessed LOCOS isolation structure using the ATHENA simulator \(^{[6,12]}\). The initial structure (top left) is formed by depositing a SiO\(_2\)/Si\(_3\)N\(_4\) structure followed by etching of this stack on the left side. The silicon is then etched to form a recessed oxide and the structure is oxidized for 90 min at 1000°C in H\(_2\)O. The time evolution of the bird's head shape during the oxidation is shown in the simulations.
Summary of Key Ideas

- Thermal oxidation has been a key element of silicon technology since its inception.

- Thermally, chemically, mechanically and electrically stable SiO₂ layers on silicon distinguish silicon from other possible semiconductors.

- The basic growth kinetics of SiO₂ on silicon are controlled by oxidant diffusion and Si/SiO₂ interface chemical reaction.

- This simple Deal-Grove model has been extended to include 2D effects, high dopant concentrations, mixed ambients and thin oxides.

- Oxidation can also have long range effects on dopant diffusion (OED or ORD) which are modeled through point defect interactions.

- Process simulators today include all these physical effects (and more) and are quite powerful in predicting oxidation geometry and properties.
Deal-Grove Model
{B.E. Deal & A.S. Grove, J. Appl. Phys. 36, 3770 (1965)}

Fisk's law about diffusion, \( \vec{J}_A = -D_{AB} \nabla C_A \)

in 1-D case \( F_z = -D \frac{\partial C}{\partial X} \sim D \cdot \frac{C_0 - C_i}{X_{ox}} \)

\[ C_0 = H \cdot P_s \]

Henry's constant

\[ \Rightarrow C_0 = H \cdot C_r \cdot k_B T \]

\[ \Rightarrow F_i = \hbar G (C_A - C_0) \]

\[ = \hbar G \left( \frac{C_A}{H k_B T} - \frac{C_0}{H k_B T} \right) \]

\[ = \hbar (C_A - C_0) \]

\( F_3 = k_s C_i \)

At steady-state \( F_i = F_2 = F_3 \),

\[ \begin{align*}
    h (C_A - C_0) &= D \cdot \frac{C_0 - C_i}{X_{ox}} \\
    h (C_A - C_0) &= k_s C_i
\end{align*} \]

\[ \begin{align*}
    X_{ox} h C_A - X_{ox} h C_0 &= D C_0 - D C_i \\
    h C_A - h C_0 &= k_s C_i
\end{align*} \]

\[ \Rightarrow \begin{align*}
    -X_{ox} h C_A + (X_{ox} h + D) C_0 &= \frac{hD}{k_s} C_A - \frac{hD}{k_s} C_0 \\
    (X_{ox} h + D + \frac{hD}{k_s}) C_0 &= X_{ox} h C_A + \frac{hD}{k_s} C_A
\end{align*} \]
\[
C_o = \frac{\chi_{ox} h C_A + \frac{h D}{k_s} C_A}{\chi_{ox} h + D + \frac{h D}{k_s}} = \frac{C_A}{1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}} (1 + \frac{k_s \chi_{ox}}{D})
\]

\[\Rightarrow C_i = \frac{h}{k_s} (C_A - C_o) = \frac{h}{k_s} C_A \left(1 - \frac{1 + \frac{k_s \chi_{ox}}{D}}{1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}}\right)\]

\[= \frac{h}{k_s} C_A \cdot \frac{\frac{k_s}{h}}{1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}}\]

\[= \frac{C_A}{1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}} \Rightarrow C_o = C_i \cdot (1 + \frac{k_s \chi_{ox}}{D})\]

\[\Rightarrow (Flux) \quad F (= F_i = F_e = F_j) = k_s \cdot C_i = \frac{k_s \cdot C_A}{1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}}\]

\[\therefore \quad F = N_i \cdot \left(\frac{d\chi_{ox}}{dt}\right)\]

\[\therefore \quad N_i \cdot \frac{d\chi_{ox}}{dt} = \frac{k_s C_A}{1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}}\]

\[\chi_{ox} \approx \frac{A}{Z} \left(\sqrt{1 + \frac{t + c}{A^2/4b}} - 1\right)\]

\[
\frac{d\chi_{ox}}{dt} = \frac{k_s \cdot C_A}{N_i \left(1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}\right)}
\]

\[N_i \int_{\chi_i}^{\chi_o} \left(1 + \frac{k_s}{h} + \frac{k_s \chi_{ox}}{D}\right) d\chi_{ox} = k_s \cdot C_A \int_0^t dt\]

\[\frac{\chi_o^2 - \chi_i^2}{B} + \frac{\chi_o - \chi_i}{B/A} = t\]

\[(Page 2)\]
\[ \beta = \frac{2Dc_A}{N_i} \quad & \quad \frac{\beta}{A} = \frac{c_A}{N_i \left( \frac{1}{k_s} + \frac{1}{h} \right)} \approx \frac{c_A k_s}{N_i} \]

\[ \frac{x^2}{B} + \frac{x}{\beta/A} = t + \tau \quad \text{with} \quad \tau = \frac{x^2 + A \chi_i}{B} \]

\[ x_0 \approx \frac{A}{z} \left( \sqrt{1 + \frac{t + \tau}{A^2/4B}} - 1 \right) \]