Text Book:
Silicon VLSI Technology
Fundamentals, Practice and Modeling
Authors: J. D. Plummer, M. D. Deal, and P. B. Griffin
Chapter 4

• A three tiered approach to control unwanted impurities in silicon
  – Clean Rooms
    • Minimize particles in the environment
  – Wafer Cleaning
    • Minimize particles on the wafers
  – Gettering
    • Minimize the effect of particles in the wafer
FRONT END PROCESSES - CLEANING, LITHOGRAPHY, OXIDATION
ION IMPLANTATION, DIFFUSION, DEPOSITION AND ETCHING

- Over the next several weeks, we'll study front end processes individually.
- Cleaning belongs to front end processes and is an important part of fabrication
- Reference - ITRS Roadmap for Front End Processes

SILICON VLSI TECHNOLOGY
Fundamentals, Practice and Modeling
By Plummer, Deal & Griffin
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Defect and Impurities

- Importance of unwanted impurities increases with shrinking geometries of devices.
- 75% of the yield loss is due to defects caused by particles (1/2 of the min feature size)
- Wafer localized light scatterers (LLS) is a starting wafer test
- Crystal originated (45-150nm) particles (COP)~1,000Å=void with SiOₓ -> affect gate oxide integrity (GOI)
- -> anneal in H₂ -> oxide decomposes and surface reconstructs! & oxide precipitates from deep depth in Si.

<table>
<thead>
<tr>
<th>Table 4-1</th>
<th>Semiconductor industry projected progress in chip size and feature size and the implications of this progress for defect size, density and contamination levels [4.1]</th>
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<tbody>
<tr>
<td>Minimum Feature Size</td>
<td>250 nm</td>
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<tr>
<td>Wafer Diameter (nm)</td>
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<td>DRAM Bits/Chip</td>
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<td>DRAM Chip Size (mm²)</td>
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<td>Maximum Wiring Levels</td>
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<td>Critical Defect Size</td>
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<td>Starting Wafer</td>
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<td>Total LLS (cm⁻²)</td>
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<td>DRAM GOI</td>
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<td>Defect Density (cm⁻²)</td>
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<td>Logic GOI</td>
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<tr>
<td>3 × 10⁸</td>
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<td>Under 1 × 10¹⁰</td>
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<td>Under 1 × 10¹¹</td>
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<tr>
<td>Under 1 × 10¹²</td>
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<tr>
<td>Under 1 × 10¹³</td>
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<td>Critical Metals on Wafer Surface After</td>
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<td>Cleaning (cm⁻³)</td>
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<td>5 × 10⁷</td>
<td>4 × 10⁷</td>
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<tr>
<td>Starting Material Recombination</td>
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<tr>
<td>Lifetime (assec)</td>
<td>≥ 300</td>
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</table>

Yield > 90% at the end requires > 99% @ each step

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Wafer Cleaning

- Surface films and doped regions must not be significantly attacked.
- Photoresist strip and particle removal typical
- Room air and process equipment delivered particles
  - Significant elements that cause severe problems in silicon include: organics, metals (Fe, Au, Cu, etc.) and alkali ions (Na, K, etc.)
Example Sensitivity

- Example #1: MOS transistor gate threshold shift

\[ V_{TH} = V_{FB} + 2\phi_f + \frac{\sqrt{2\varepsilon_S q N_A (2\phi_f)}}{C_O} + \frac{qQ_M}{C_O} \quad (1) \]

- \( Q_M \) is the mobile charge density (number of charges per cm\(^2\)) of Na\(^+\) and K\(^+\) in the gate oxide

If \( t_{ox} = 10 \) nm, then a 0.1 volt \( V_{th} \) shift can be caused by
\( Q_M = 6.5 \times 10^{11} \) cm\(^2\) (< 0.1% monolayer or 10 ppm in the oxide).

- Prevented MOS technologies initially from being important commercially!
Example Sensitivity

- Example #2: MOS DRAM
  - Storage of charge based on minimal charge leakage in time.
    - Refresh required to maintain charges after a technology defined period of time.
  - Dominated by Shockley, Reed Hall (SRH) recombination (intermediate impurity related energy levels).
    - $\sigma$ is the trap cross sectional area, $(10^{-15}\text{cm}^{-2}) v_{th}$ is the minority carrier thermal velocity $(10^7 \text{ cm/sec})$, and $N_t$ is the density of traps.
    - Deep-level traps (Cu, Fe, Au etc.) Pile up at the surface where the devices are located.

\[ \tau_R = \frac{1}{\sigma \cdot v_{th} \cdot N_t} \approx 100 \mu\text{sec} \]  

- Refresh time of several msec requires a generation lifetime of

\[ \tau_R = \frac{1}{\sigma \cdot v_{th} \cdot N_t} \approx 100 \mu\text{sec} \]  

- This requires $N_t \approx 10^{12} \text{ cm}^{-3}$ or $\approx 0.02 \text{ ppb}$ (see text).
Example: The Role of Surface Cleaning in Processing

Residual contaminants, layers affect kinetics of processes.

Surface effects are very important (MORE) in scaled down devices.
# 2003 ITRS Front End Processes

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<td>Technology Node (half pitch)</td>
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<td>180 nm</td>
<td>130 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
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<td>35 nm</td>
<td>25 nm</td>
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<td>1G</td>
<td>4G</td>
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<td>Critical Defect Size</td>
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<td>90 nm</td>
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<td>45 nm</td>
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<td>&lt;0.35</td>
<td>&lt;0.35</td>
<td>&lt;0.35</td>
<td>&lt;0.35</td>
<td>&lt;0.35</td>
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<td>Starting Wafer Total Bulk Fe (cm⁻²)</td>
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<td>1x10⁷</td>
<td>1x10⁷</td>
<td>1x10⁷</td>
<td>1x10⁷</td>
<td>1x10⁷</td>
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<td>Metal Atoms on Wafer Surface After Cleaning (cm⁻²)</td>
<td>5x10⁷</td>
<td>1x10⁷</td>
<td>1x10⁶</td>
<td>1x10⁵</td>
<td>1x10⁵</td>
<td>1x10⁵</td>
<td>1x10⁵</td>
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<tr>
<td>Particles on Wafer Surface After Cleaning (μm/wafer)</td>
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<td>80</td>
<td>86</td>
<td>195</td>
<td>106</td>
<td>168</td>
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### ITRS 2007 Ed. Front End Processes

**Table FEP2a: Starting Materials Technology Requirements—Near-term Years**

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<td>57</td>
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<td>MPU 45C Metal 1 (M1) Pitch (nm)</td>
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<td>DRAM Total Chip Area (mm²)</td>
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<td>DRAM Active Transistor area (mm²)</td>
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<td>18.2</td>
<td>15.1</td>
<td>12.1</td>
<td>10.1</td>
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<td>80</td>
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<td>21.7</td>
<td>17.1</td>
<td>13.1</td>
<td>10.0</td>
<td>8.0</td>
<td>6.9</td>
</tr>
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**Maximum Substrate Diameter (mm)—High-volume Production (>500 wafers starts per month)**

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<th>300</th>
<th>300</th>
<th>300</th>
<th>300</th>
<th>300</th>
<th>450</th>
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<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
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**Visible particles (µm), latest sphere equivalent (A)**

<table>
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<tr>
<th>265</th>
<th>265</th>
<th>265</th>
<th>265</th>
<th>265</th>
<th>245</th>
<th>245</th>
<th>245</th>
<th>232</th>
</tr>
</thead>
</table>

**Residual defects, SFQ, Minimum Site Size (mm²) Site Size**

<table>
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<tr>
<th>565</th>
<th>557</th>
<th>554</th>
<th>548</th>
<th>536</th>
<th>532</th>
<th>528</th>
<th>525</th>
</tr>
</thead>
</table>

**Epitaxial Wedge ± (95% Chip Yield)**

| 0.011 | ≤ 0.014 | ≤ 0.017 | ≤ 0.011 | ≤ 0.014 | ≤ 0.017 | ≤ 0.011 | ≤ 0.014 | ≤ 0.017 |

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Clean Factories – Wafer Fab Facility

- The wafer fabrication area “Clean Rooms” must be particle free.
  - Sources of particles
    • Air (normal presence of particles) and Water
    • Machinery – particularly due to friction, metals
    • People – 5 to 10 million particles per minute, organic
    • Supplies – brought in to room for use
    • Processing
  - Rooms and People
    • Clean room limited access, finger wall machine access
    • Bunny suits, gloves, air showers, covered faces/facemask
    • Glove box and robots
  - Air handling
    • Positive air pressure, HEPA filters
Stanford’s CIS Clean Room

- The 10,500 square feet clean room is vibration-isolated from the rest of the building. Support equipment, such as chilled water, vacuum pumps, air compressors, and acid waste neutralizers, are located in the basement. Corrosive and toxic gases are in a monitored gas area. Liquid gas storage tanks, emergency power generators, and a de-ionized water plant are outdoors.

- Every 8 seconds, the entire air volume of this room is circulated out to large air ducts, like the meter-wide duct just behind the glass. From there the air flows up to the third floor, down through filters on the second floor, and then back into the clean room through the ceiling.

- People inside the room wear bunny suits to minimize the release of human particles into the air. The result is that each cubic foot of air has fewer than 100 particles of size 500 nanometers (Class 100), much cleaner than the air in a hospital operating room.

- [http://www-cis.stanford.edu/~marigre/CleanRoom.html](http://www-cis.stanford.edu/~marigre/CleanRoom.html)
- [http://snf.stanford.edu/Education/VirtualTour.html](http://snf.stanford.edu/Education/VirtualTour.html)
Level 1 Contamination Reduction: Clean Factories

- Air quality is measured by the “class” of the facility.
  - Less than X total particles greater than 0.5 um per cubic foot of air.

Factory environment is cleaned by:
- HEPA filters (99.07% eff.)
- Air recirculation (laminar >50 cm/sec)
- Bunny suits for workers
- Filtration of chemicals and gases
- Manufacturing protocols

(Photo courtesy of Stanford Nanofabrication Facility.)
Wafer Cleaning

- Remove particles, films such as photoresist, and any other trace contaminants
- Distinct processes
  - Silicon wafer clean (frontend processes)
  - Post metalization clean (backend processes)
- Frontend Wafer Cleaning based on RCA process
  - RCA was originally the Radio Corporation of America
  - Werner Kern developed the basic procedure in 1965 while working for RCA.
- The RCA clean involves the following:
  1. Removal of the organic contaminants (Organic Clean)
  2. Removal of thin oxide layer (Oxide Strip)
  3. Removal of ionic contamination (Ionic Clean)
The RCA Clean

- The first step (called SC-1, where SC stands for Standard Clean) is performed with a 1:1:5 solution of NH$_4$OH + H$_2$O$_2$ + H$_2$O at 70° to 80° C for 10 minutes.
  - This treatment oxidizes organic films and complexes Group IB and IIB metals as well as Au, Ag, Cu, Ni, Zn, Cd, Co, and Cr. The solution dissolves and regrows a thin native oxide layer on the silicon.
- The next step is a short immersion in a 1:50 solution of HF + H$_2$O at 25° C
  - Remove the thin oxide layer and some fraction of ionic contaminants.
- Perform a DI rinse.
- The next step (called SC-2) is performed with a 1:1:6 solution of HCl + H$_2$O$_2$ + H$_2$O at 70° to 80° C for 10 minutes.
  - This treatment removes alkali ions and cations (Al, Fe, Mg) that form NH$_3$OH insoluble hydroxides in solutions like SC-1. In SC-2 they for soluble complexes. This solution also completes the removal of metal contaminants.
- Perform a DI rinse.
Level 2 Contamination Reduction: Wafer Cleaning

- **Organic Clean**
  - RCA clean is “standard process” used to remove organics, heavy metals and alkali ions.
  - Ultrasonic agitation is used to dislodge particles.
De-Ionized (DI) Water

- Clean water for silicon processing

- DI Water conductivity example:

\[ \text{DI water is necessary: } \text{H}_2\text{O} \leftrightarrow \text{H}^+ + \text{OH}^- \]

\[
\text{Diffusivity of: } \begin{align*}
\text{H}^+ & \approx 9.3 \times 10^{-5} \text{ cm}^2\text{s}^{-1} \\
\text{OH}^- & \approx 5.3 \times 10^{-5} \text{ cm}^2\text{s}^{-1}
\end{align*}
\]

\[ \text{with } [\text{H}^+] = [\text{OH}^-] = 6 \times 10^{-13} \text{ cm}^3 \]

\[ \rightarrow \mu_{\text{H}^+} = qD/kT = 3.59 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \]

\[ \rightarrow \mu_{\text{OH}^-} = qD/kT = 2.04 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \]

\[ \rho = \frac{1}{q([\text{H}^+]\mu_{\text{H}^+} + [\text{OH}^-]\mu_{\text{OH}^-})} = 18.5 \text{ M}\Omega\text{cm} \]

Distilled water is typically 10 uS/cm or 0.1 M\Omega cm
Gettering

- Removing trace elements from active transistor locations by causing them to combine with defects in the silicon.
  - Active devices cover a very small portion of the silicon volume, typically near one surface.
  - Metals and alkali ions have very high diffusivity.
  - They tend to be easily captured either in regions with mechanical defects or in regions which chemically trap them.
- For the alkali ions, gettering generally uses dielectric layers on the topside (PSG or barrier Si3N4 layers).
- For metal ions, gettering generally uses traps on the wafer backside (extrinsic) or in the wafer bulk (intrinsic).
Level 3 Contamination Reduction: Gettering

Elements for gettering:
- Alkali Ions
- Metals

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Gettering

- Steps:
  1. Free elements from current sites, making them mobile
  2. Diffuse through silicon to desired sites
  3. Become trapped.
- Aalkali ions: dielectric layers on the topside (PSG or barrier Si3N4 layers).
- Heavy metal ions: traps on the wafer backside (extrinsic) or in the wafer bulk (intrinsic).
Gettering

- Diffusivity of various elements
  - Diffuse as interstitials (they don’t easily fit in the lattice)
    (through wafer during normal dopant drive-in)
  - Dopants diffuse as a substitution
- “Trap” sites can be created by SiO₂ precipitates (intrinsic gettering), or by backside damage (extrinsic gettering).

- In intrinsic gettering, CZ silicon is used and SiO₂ precipitates are formed in the wafer bulk through temperature cycling at the start of the process.
Intrinsic Gettering: Oxide Precipitates

Precipitates (size) grow @ high T

Density of nucleation sites grow @ low T

The largest & the most dense defects -> the most efficient gettering

Surface (top) has few defects.
MEASUREMENT METHODS
Measurement Methods

- Clean factories = particle control
  - Detect concentrations < 10/wafer of particles smaller than 0.1 μm

- Unpatterned wafers (blank)
  - Count particles in microscope
  - Laser scanning systems → maps of particles down to ≈ 0.2 μm
  (see MEMC video on laser inspection from Chapter 3)

- Patterned wafers
  - Optical system compares a die with a “known good reference”
    die (adjacent die, chip design - its appearance)
  - Image processing identifies defects (SEM)
  - Test structure (not in high volume manufacturing)
Test Structures

Resistance

Capacitance

Trapped charge
\( Q_T \rightarrow V_{TH} \) change

Dielectric breakdown due to particles, metals etc.

Figure 6-14 (layout top view) of a typical electrical test structure designed to detect defects in an interconnect layer. Typical open and short defects are illustrated.

Figure 6-15 MOS capacitor test structure. The voltage applied to the gate is ramped up until significant current flows through the gate dielectric. The electric field at which this breakdown occurs is plotted on the right.
Monitoring the Wafer Cleaning Efficiency

Concentrations of impurities determined by surface analysis

- Excite
- Identify (unique atomic signature)
- Count concentrations

He$^+$ 1-3 MeV
Rutherford Back-scattering

Secondary Ion Mass Spectrometry: O$^+$ or Cs$^+$ sputtering and mass analyses

Figure 4-16: Surface analysis techniques used to identify and quantify contamination in IC manufacturing.

Primary beam –
- e$^-$
- e$^-$
- X-ray
- ions (SIMS)
- ions (RBS)

good lateral resolution

good depth resolution and surface sensitivity

poor depth resolution and poor surface sensitivity

excellent

good depth resolution, reasonable sensitivity (0.1 atomic%)
Electron Beam Emissions (1)

Elastic collision of incoming electrons with atoms (reflected back) ~ the same energy as for the incoming electrons

\[ \text{Figure 4-17} \quad \text{Energy distribution of electrons emitted from a solid under electron bombardment.} \]
Electron Beam Emissions (2)

- If X-Ray is at the input:
  - el. Emitted≠ X-ray Photoelectron Spectroscopy (XPS)
  - X-ray emitted≠ X-ray Fluorescence (XRF)

XPS usually more dominant for lighter elements, XRF for heavier

The core electron energy levels

- AES scheme is for lighter elements (Z<33 as is crossover between Auger/AES and X-Ray/XES)

Figure 4-18: Band diagram representation of some of the processes used in surface analytical methods.
Monitoring of Gettering Through Device Properties and Dielectric

- p-n leakage, refresh time DRAM junction and dielectric breakdown, β of n-p-n emission-capture
- Material properties: τ_0 (>> τ_R) in the bulk and on the surface

**Photoconductive Decay** Measurements

\[ \Delta n = g_{op} \tau_G \]

- Carriers are generated due to light
- Decrease resistivity
- Recombine

\[ \Delta n(t) = \Delta n(0) \exp\left(-t / \tau_R\right) \]
Carrier Generation Lifetime

Deep Depletion - Return to Inversion via Carrier Generation (measure $\tau_G$) and surface recombination (s)

Zernst technique:

$$\frac{d}{dt} \left( \frac{C_{ox}}{C} \right)^2 \rightarrow \tau_G$$

$$s = f(N_A, \sigma)$$

$\sigma$ - Capture cross section

if plotted vs. $(C_{ox}/C) - 1$
Lifetime Measurements: Open Circuit Voltage Decay

\[ V_D(t) = V_D(0) - kT \ln(\text{erf} \left( \frac{I}{s} \right)) \]

Diode switched from ON \( V_D \) when carriers recombine

for \( V < 4 \)

\[ \tau_n = \frac{kT/q}{dV_D/dt} \]

Measurements include surface and bulk recombination

Use also DLTS:
- Identifies traps \( (E_t) \) and concentrations
- Thermal or photoexcitation processes in voltage modulable space-charge region
- (Schottky Diode, p-n junction, MOS Capacitor)
- Measured: capacitance, currents or conductance
Deep Level Transient Spectroscopy

• An experimental tool for studying electrically active defects (known as charge carrier traps) in semiconductors.
  - DLTS enables to establish fundamental defect parameters and measure their concentration in the material.
  - Some of the parameters are considered as defect “finger prints” used for their identifications and analysis.
  - identifies traps (Et) and concentrations

• Thermal or photoexcitation processes in voltage modulable space-charge region (Schottky Diode, p-n junction, MOS Capacitor)
  - Measured: capacitance, currents or conductance
Models and Simulation Goal

Computer Integrated Manufacturing (CIM)
- Tools to monitor and control machines, to maintain recipes, to control wafer throughput, and to improve operating efficiency (i.e. higher yields)
- Higher initial yields and shorter time to maturity.

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<td>Minimum Feature Size (nm)</td>
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<td>Wafer Diameter (mm)</td>
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<td>300</td>
<td>300</td>
<td>450</td>
<td>450</td>
</tr>
<tr>
<td>DRAM Bits/Chip</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
<td>256G</td>
</tr>
<tr>
<td>Initial Yield Level (%)</td>
<td>25</td>
<td>50</td>
<td>80</td>
<td>85</td>
<td>88</td>
<td>90</td>
</tr>
<tr>
<td>Time to Mature Yield Level (years)</td>
<td>4</td>
<td>3</td>
<td>1</td>
<td>0.8</td>
<td>0.6</td>
<td>0.5</td>
</tr>
</tbody>
</table>
Contamination and Yield

- ≈ 75% of yield loss in modern VLSI fabs is due to particle contamination.
- Yield models depend on information about the distribution of particles.
- Particles on the order of 0.1 - 0.3 μm are the most troublesome:
  - larger particles precipitate easily
  - smaller ones coagulate into larger particles
Contamination and Yield Model

- Yields are described by Poisson statistics in the simplest case.
  \[ Y = \exp^{-A_c D_o} \]
  where \( A_c \) is the critical area and \( D_o \) the defect density.
- If some fraction of the wafer, \( G \), always produces zero yields (near the edge of the wafer) this is modified as
  \[ Y = (1 - G) \cdot \exp^{-A_c D_o} \]
- This model assumes independent randomly distributed defects and often under predicts yields.
Alternate Models

- Use of negative binomial statistics eliminates these assumptions and is more accurate.

\[ Y = \frac{1}{\left(1 + \frac{A_c D_0}{C}\right)^C} \quad (4) \]

- where C is a measure of the particle spatial distribution (clustering factor).

\[ D_0 = 1 \text{ cm}^{-2} \]

\[ \text{Chip Area (cm}^2) \]

\[ 0.0001 \quad 0.001 \quad 0.01 \quad 0.1 \quad 1 \]

Poisson

Negative Binomial (C = 10)

Negative Binomial (C = 2)
Negative Binomial Yield for C=2

- Vertical lines are estimated chip sizes (from the ITRS).
- Note that defect densities will need to be extremely small in the future to achieve the high yields required for economic IC manufacturing.
- (See particle defect densities on Table 4-1.)
Overall Yield

- The total wafer yield must be the product of the yields for each process step.

\[ Y = \prod_{i=1}^{\text{levels}} \left( 1 + \frac{A_{Ci}D_{Oi}}{Ci} \right)^{-Ci} \]

- Note that previous curves refer to chip yield
  - Table 4-1 and Figures 4-22 and 4-23
Modeling Wafer Cleaning

- Cleaning involves removing particles, organics (photoresist) and metals from wafer surfaces.
  - Particles are largely removed by ultrasonic agitation during cleaning.
  - Organics like photoresists are removed in an \( O_2 \) plasma or in \( H_2SO_4/H_2O_2 \) solutions.
  - The “RCA clean” is used to remove metals and any remaining organics.

- Metal cleaning can be understood in terms of:
  - Convert metal into ions soluble in the cleaning solution
    - Oxidation: the process that removes electrons from an atom (\( \rightarrow \))
    - Reduction: the process that gains and electron (\( \leftarrow \))

\[
\text{Si} + 2\text{H}_2\text{O} \leftrightarrow \text{SiO}_2 + 4\text{H}^+ + 4\text{e}^- \quad (5)
\]
\[
\text{M} \leftrightarrow \text{M}^{z+} + ze^- \quad (6)
\]
Modeling Wafer Cleaning

\[ Si + 2H_2O \leftrightarrow SiO_2 + 4H^+ + 4e^- \quad (5) \]
\[ M \leftrightarrow M^{z+} + ze^- \quad (6) \]
\[ 2H_2O \leftrightarrow H_2O_2 + 2H^+ + 2e^- \quad (7) \]

- If we have a water solution with a Si wafer and metal atoms and ions, the stronger reaction will dominate.
- Generally (7) is driven to the left and (5) and (6) to the right so that SiO_2 is formed and M^{z+} is a solution soluble ion.
- Good cleaning solutions drive (6) to the right since M^{z+} is soluble and will be desorbed from the wafer surface.
- No model exists, but there is a general understanding of the chemistry.
### Oxidation-Reduction Reactions

<table>
<thead>
<tr>
<th>Oxidant/Reductant</th>
<th>Standard Oxidation Potential (volts)</th>
<th>Oxidation-Reduction Reaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mn^{2+}/Mn</td>
<td>1.05</td>
<td>Mn ↔ Mn^{2+} + 2e^-</td>
</tr>
<tr>
<td>SiO_2/Si</td>
<td>0.84</td>
<td>Si + 2H_2O ↔ SiO_2 + 4H^+ + 4e^-</td>
</tr>
<tr>
<td>Cr^{3+}/Cr</td>
<td>0.71</td>
<td>Cr ↔ Cr^{2+} + 3e^-</td>
</tr>
<tr>
<td>Ni^{2+}/Ni</td>
<td>0.25</td>
<td>Ni ↔ Ni^{2+} + 2e^-</td>
</tr>
<tr>
<td>Fe^{3+}/Fe</td>
<td>0.17</td>
<td>Fe ↔ Fe^{3+} + 3e^-</td>
</tr>
<tr>
<td>H_2SO_4/H_2SO_3</td>
<td>-0.20</td>
<td>H_2O + H_2SO_3 ↔ H_2SO_4 + 2H^+ + 2e^-</td>
</tr>
<tr>
<td>Cu^{2+}/Cu</td>
<td>-0.34</td>
<td>Cu ↔ Cu^{2+} + 2e^-</td>
</tr>
<tr>
<td>O_2/H_2O</td>
<td>-1.23</td>
<td>2H_2O ↔ O_2 + 4H^+ + 2e^-</td>
</tr>
<tr>
<td>Au^{3+}/Au</td>
<td>-1.42</td>
<td>Au ↔ Au^{3+} + 3e^-</td>
</tr>
<tr>
<td>H_2O_2/H_2O</td>
<td>-1.77</td>
<td>2H_2O ↔ H_2O_2 + 2H^+ + 2e^-</td>
</tr>
<tr>
<td>O_3/O_2</td>
<td>-2.07</td>
<td>O_2 + H_2O ↔ O_3 + 2H^+ + 2e^-</td>
</tr>
</tbody>
</table>

- The strongest oxidants are at the bottom (H_2O_2 and O_3). These reactions go to the left grabbing e^-, dominating, and forcing (6) to the right.
- Fundamentally the RCA clean works by using H_2O_2 as a strong oxidant.
Modeling Gettering

- Gettering consists of:
  1. Making metal atoms mobile.
  2. Migration of these atoms to trapping sites.
  3. Trapping of atoms.

- Step 1 generally happens by “kicking-out” the substitutional atom into an interstitial site. One possible reaction is:
  \[ \text{Au}_s + I \leftrightarrow \text{Au}_i \]

- Step 2 usually happens easily once the metal is interstitial since most metals diffuse rapidly in this form.

- Step 3 happens because heavy metals segregate preferentially to damaged regions or to N\textsuperscript{+} regions or pair with effective getters like P (AuP pairs).
Gettering

All metal atoms mobile ($D_{M_i} > D_{M_S}$, 10x)

Except of Ti, Mo, etc.

$D_M >> D_{Dopants}$

Sol. Sol. $M_S >> M_S$ (Cu, Ni)

Sol. Sol. $M_i << M_S$ (Au, Pt)

$Au_S + I \leftrightarrow Au_i$ kick-out mechanism, then getter

$Au_S \leftrightarrow Au_i + V$ dissociative or Frank-Turnbull mech.

$I$ increase improves gettering of $Au$

$V$ increase hinders gettering

Ex. P diffusion, Ion Implant=damage, intrinsic gettering (=I↑)
Metal Diffusion to the Gettering Sites

**Figure 4-25** General shape of Au outdiffusion profiles if simple outdiffusion dominates the gettering process. Starting with a flat profile ($10^{18}$ cm$^{-3}$), the concentration drops off with time through the wafer as the Au diffuses to the back surface (left side). This simulation was done with Silvaco’s SSUPREM IV, a process simulator we will discuss in more detail in later chapters.

**Figure 4-26** Experimental 1000°C Au outdiffusion profiles during gettering to the wafer backside. (After [4.51].)
Trapping the Metal Atoms at the Gettering Sites (1)

- Trapped by: ion implantation, P diffusion, laser damage, poly-Si films, mechanical damage, etc. But HOW?

- Physical damage -> metal trapped at defect sites; binding energy $E_g$ depends on $T$.

  \[
  \text{Fraction Bound} = (1 - K_1 \exp \frac{-E_g}{kT})
  \]

- Segregation, related to solubility in the silicon perfect crystal and in the gettering region

  \[
  \begin{align*}
  C_{\text{Au, Si}} &= N_S \exp \left( -E_{A1}/kT \right) & \text{in silicon region} \\
  C_{\text{Au, G}} &= N_G \exp \left( -E_{A2}/kT \right) & \text{in gettering region}
  \end{align*}
  \]

- The segregation coefficient is defined as

  \[
  k_0 = (C_{\text{Au, G}} + C_{\text{Au, Si}})/C_{\text{Au, Si}} = 1 + K_2 \exp \left[ -(E_{A1} - E_{A2})/kT \right]
  \]

  For the case of phosphorous

  \[
  k_0 = 1 + N_G/5 \times 10^{22} \exp (0.82 \text{eV}/kT)
  \]  (fraction of Au bound in gettering)
Trapping the Metal Atoms at the Gettering Sites (2)

- Enhances sol.sol by high dopant concentrations: in “n” Au=acceptor, “p” - Au=donor
  \[ \text{Au} + e^- \leftrightarrow \text{Au}^+ \]
  \[ K_{eq} = \frac{[\text{Au}^+]}{[\text{Au}][e^-]} \text{= constant} \]
  \[ \frac{[\text{Au}^+]}{[\text{Au}]} n_i = \frac{[\text{Au}^+]}{[\text{Au}]} n \text{ or } \frac{[\text{Au}^+]}{[\text{Au}]} n = n_i \]
  Au acceptor ↑ in “n” Si (100x if \( n_i(1000^\circ C) = 7.4 \times 10^{18} \) → \( 10^{21} \) cm\(^3\) doping level)

- Ion pairing model: \( \text{AuP} \leftrightarrow \text{less strain} \)
- Coulombic attraction: \( \text{Au} + \text{P} \rightarrow \text{AuP}^- \)

- Interaction with point defects \( V \leftrightarrow \text{in “n”} \)
  \( \text{Au}^+ + V^- \leftrightarrow \text{Au}_x \text{ at the trapezd site} \)

- Intrinsic gettering - trapping on dislocations and SF which surround precipitates.

Dislocations have compressive and tensile stress - accommodate smaller and larger atoms
Limits and Future Trends in Technology and Modeling (1)

• Eliminate defects from wafers: particles, contaminants, clean room.
  – SMIF Box (Standard Mechanical Interface): limit clean room size, transport between stations in a clean box

• Wafer cleaning (next slide)

• Gettering:
  – intrinsic (less extrinsic),
  – control $O_p$, $C_s$,
  – use low T processing,
  – use modeling tool $\rightarrow$ point defects engineering,
  – release, diffuse, entrap.
Limits and Future Trends in Technology and Modeling (2)

- Wafer cleaning in future ICs
  - less chemicals (liquids, vapors), more diluted (disposal)
  - New cleaning:
    - Use ozone
    - Dry and vapor phase, (Vapors, Plasmas) environment! Cluster tools
    - Low Energy Physical Processes (sputtering)
    - Photochemically enhanced clean

Figure 4-29 Possible room temperature cleaning procedure replacement for the RCA clean (4.28).
Summary of Key Ideas

- A three-tiered approach is used to minimize contamination in wafer processing.
- Particle control, wafer cleaning and gettering are some of the "nuts and bolts" of chip manufacturing.
- The economic success (i.e. chip yields) of companies manufacturing chips today depends on careful attention to these issues.
- Level 1 control - clean factories through air filtration and highly purified chemicals and gases.
- Level 2 control - wafer cleaning using basic chemistry to remove unwanted elements from wafer surfaces.
- Level 3 control - gettering to collect metal atoms in regions of the wafer far away from active devices.
- The bottom line is chip yield. Since "bad" die are manufactured alongside "good" die, increasing yield leads to better profitability in manufacturing chips.
ECE 541/ME 541
Microelectronic Fabrication Techniques

MW 4:00-5:15 pm, Taft Hall 204

Introduction to Cleanroom

Zheng Yang

ERF 3017, email: yangzhen@uic.edu
Semiconductor manufacture particulate contamination.

A 2µ x 2µ molecular contaminant captured on KLA-Tencor 8100 CD SEM at 75kX magnification.

A 6µ x 6µ molecular contaminant captured on KLA-Tencor 8100 CD SEM at 25kX magnification

A 2µ x 2µ molecular contaminant captured on KLA-Tencor 8100 CD SEM at 75kX magnification
The nature of particulate contamination....continued.
Environmental Abundancy

- The smaller the diameter, the more aerosols are there!
- The smaller the structures, the harder it is to provide a clean environment.

Particles

- Contaminants - particulate larger than 1/10th feature size
- Killer defects - particles located in critical part of device that destroy its functioning
Federal Standard 209E

The number of 0.5µm-diameter-particles in 1 m³:

<table>
<thead>
<tr>
<th>MEASURED PARTICLE SIZE (MICROMETERS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLASS</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>100</td>
</tr>
<tr>
<td>1,000</td>
</tr>
<tr>
<td>10,000</td>
</tr>
<tr>
<td>100,000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Environment</th>
<th>Class Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULSI Fab</td>
<td>1</td>
</tr>
<tr>
<td>VLSI Fab</td>
<td>10</td>
</tr>
<tr>
<td>VLF station</td>
<td>100</td>
</tr>
<tr>
<td>Public Halls</td>
<td>1000-10000</td>
</tr>
<tr>
<td>House Room</td>
<td>100000</td>
</tr>
<tr>
<td>Outdoors</td>
<td>&gt;500000</td>
</tr>
</tbody>
</table>
Airborne particulate cleanliness, English system, Fed. Std. 209E

Chart gives maximum number of particles in a given size range per cubic foot.

<table>
<thead>
<tr>
<th>Class</th>
<th>(0.1\mu)</th>
<th>(0.2\mu)</th>
<th>(0.3\mu)</th>
<th>(0.5\mu)</th>
<th>(5\mu)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.50E+01</td>
<td>7.50E+00</td>
<td>3.00E+00</td>
<td>1.00E+00</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>3.50E+02</td>
<td>7.50E+01</td>
<td>3.00E+01</td>
<td>1.00E+01</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td>7.50E+02</td>
<td>3.00E+02</td>
<td>1.00E+02</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td></td>
<td></td>
<td>1.00E+03</td>
<td>7.00E+00</td>
</tr>
<tr>
<td>10000</td>
<td></td>
<td></td>
<td></td>
<td>1.00E+04</td>
<td>7.00E+01</td>
</tr>
<tr>
<td>100000</td>
<td></td>
<td></td>
<td></td>
<td>1.00E+05</td>
<td>7.00E+02</td>
</tr>
</tbody>
</table>

![Graph showing the number of particles per cubic foot vs. particle size (micron)]
Metric classification of airborne particulate cleanliness (Fed. 209e).
**SIA Roadmap for particulate contamination.**

<table>
<thead>
<tr>
<th>Year of First Product Shipment Technology Node</th>
<th>1997 250 nm</th>
<th>1999 180 nm</th>
<th>2002 130 nm</th>
<th>2005 100 nm</th>
<th>2008 70 nm</th>
<th>2011 50 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Environment Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Critical particle size (nm) (A)</td>
<td>125</td>
<td>90</td>
<td>65</td>
<td>50</td>
<td>35</td>
<td>25</td>
</tr>
<tr>
<td>Particles ^3 crit size (m(^3)) (B)</td>
<td>27</td>
<td>12</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Mechanism for particulate filtration.

Figure 1: Particle collection mechanisms

- Inertial impact
- Diffusion
- Electrostatic attraction
- Interception
- Flow streamlines
- Gravity
Filtration efficiency.

Figure 3: Efficiency as a function of fiber diameter

Figure 4: Efficiency as a function of gas velocity.
Filtration efficiency.
Construction of HEPA filter.

Standard HEPA filter size 60 cm × 120 cm

Sealant: a non-Newtonian fluid ensures a lasting seal

Laminar air flow

Sheet metal skirts minimize fluid displacement

Extruded aluminum channels support the filters
HEPA filter construction.

- Filter frame
- Channel filled with fluid seal
- Continuous sheet of corrugated filter medium
- Adhesive bond between filter pack and integral frame
HEPA filter construction...alternate design.
HEPA filters: examples.
Examples of HEPA filtration.

Before filtration.  

After filtration.
Cleanroom Evolution

Dry

Wet

VLF (Vertical Laminar Flow) Hoods (1970’s)
Also HLF existent
Stand next to each other to pass wafers along inside
Back to the Ballroom Design

Back to the Ballroom Design because of more processing steps and more stations. Air Circulation at low speed. (1990’s)
Conventional cleanroom technology: The ballroom concept.
Conventional cleanroom technology: Flow diagram.
Conventional cleanroom: Air supply area.
Cleanroom technology: Mini-environment concept.
Implementation of mini-environment concepts.

Integrated mini-environment required on all tools

- Integrated mini-environment
- Facility supplied mini-environment

- Class 100(T)
- No gap between FOP and the loadport during wafer process
- Baywall Air intake
- Fan Final filter
- Equipment body (process & metrology equipment)
- Raised Floor
- Adjustable dampers are required

- OHT
- Wafer handling zone
- Air duct connection
- Pre-filter?
Smif Pods and Mini-Environments

Mid 1980’s developed by HP (Agilent)
Mini-Environment System

place in non-temperature-controlled baths, and rely on the room temperature.

Figure 5.14  Mini-environment system elements.

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Mini-environments... example.
Transporting Wafers

Foster and Pillai

Figure 1 200 mm and 300 mm wafer carrier comparison.

Table 1 Metrics for silicon wafers

<table>
<thead>
<tr>
<th>Wafer Metrics (nominal)</th>
<th>200 mm wafers</th>
<th>300 mm wafers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer thickness at center (µm)</td>
<td>725</td>
<td>775</td>
</tr>
<tr>
<td>Single wafer weight (gm)</td>
<td>53</td>
<td>128</td>
</tr>
<tr>
<td>Weight of 13 wafers (gm)</td>
<td>689</td>
<td>1664</td>
</tr>
<tr>
<td>Weight of 25 wafers (gm)</td>
<td>1325</td>
<td>3200</td>
</tr>
<tr>
<td>Applicable SEMI Standards</td>
<td>M 1</td>
<td>M1.5; M 28</td>
</tr>
</tbody>
</table>
Measurements of particulate contamination

**Particle Measuring Systems model 7625**
Condensation particle counter.
Detectible particle size: 20nm.
Concentration range: 2000 particles/sec.
Concentration range: $10^6$ particles/ft.$^3$. 
Condensation particle counter...example.

Biral scanning mobility particle Sizer.
Beta attenuation counters.

The Model BAM 1020, Beta-Attenuation Mass Monitor,
Light scattering geometry

Figure 2

Light extinction geometry

Figure 3
Do’s and Don’t’s
Clothing for semiconductor manufacturing environment.

<table>
<thead>
<tr>
<th>Class 100,000</th>
<th>Class 10,000</th>
<th>Class 1,000</th>
<th>Class 100</th>
<th>Class 10</th>
<th>Class 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>MATERIAL</td>
<td>TYVEK®</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEAMS</td>
<td>SERGED SEAM</td>
<td>BOUND SEAM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PACKAGING</td>
<td>BULK PACKAGED</td>
<td>CLEANED</td>
<td>STERILE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GARMENT TYPES</td>
<td>HAIR COVERING, HOOD, FROCK, SHOE COVERS, GLOVES</td>
<td>HOOD, FACIAL COVERING, COVERALL, BOOT COVERS, GLOVES</td>
<td>HOOD, COVERALL, BOOT COVERS, GLOVES</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Entering the Cleanroom

- Adhesive Floor Mats
- Gowning Area
- Air Pressure Issues
- Shoe Cleaner
- Glove Cleaner
- Air Shower
- Double Door Pass Through
- Static Control
Clothing for clean room: Bunny Suits
Gowning Procedure

1. Upon entering gowning area, step on the sticky mat with both feet several times.

2. Put shoe covers over your street shoes.
3. Wash hands thoroughly.

4. Sterile Gloves are donned in an aseptic manner and should extend part way up the arm.
6. Retrieve garments.

6. Make sure facemask fits snuggly and bouffant covers all hair.
7. Put on hood, make sure face mask is on the bridge of the nose.

8. Adjust hood using snaps on the back.
9. Gather coverall at waist level.

10. Make sure suit does not touch the floor while putting it on.
13. Zip coverall up and snap around neck.

14. Snap coverall leg cuffs.
15. Put on boots and adjust top of boot to fit tightly around calf and snap.

16. Snap back of boot to coverall leg.
17. Once each boot is donned, cross over to the aseptic side of your gown room.

18. Don sterile gloves over Gowning gloves.
19. Don Sterile Goggles after having fully gowned, check yourself in the mirror to ensure that everything fits properly with no gaps.

20. Exit the gowning room toward the cleanroom.
Static Control

![Diagram of static control system](image)

---

Air  | Human Skin  | Glass  
---|---|---
Human Hair  | Nylon  | Wool  
Lead  | Aluminium  | Paper  
Steel  | Cotton  | Steel  
Hard Rubber  | Nickel-copper  | Brass-silver  
Synthetic Rubber  | Polyurethane  | Polypropylene  
PVC  | Silicon  | Teflon  

Increasingly Positive  

Increasingly Negative

Figur

(Hy, Han

Page 46
Wafer Cleaning

Etch:
SC-1 Removes Organics
SC-2 Removes Alkali Ions, Hydroxides, Metal Complexes
10 Times more diluted they also work fine
Wafer Cleaning

1. NH₃ + H₂O₂
2. HF
3. HCl + H₂O₂

Most wafer manufacturers use a final cleaning method developed by RCA in 1970. The 3-step process starts with a solution of ammonia, hydrogen peroxide and RO/DI water to remove organic impurities and particles from the wafer surface. Next, natural oxides and metal impurities are removed with hydrofluoric acid, and finally, a solution of hydrochloric acid and hydrogen peroxide causes clean new natural oxides to grow up on the surface.
Cryocleaning

CO₂ expands and cools down, which ablates dust more efficiently than ‘compressed air’
**Water Flow Rinsing**

Controlled flow direction prevents contamination to come from one wafer to the next.
Spray-Dump Rinsing

The surface of any liquid is usually much dirtier than its bulk. Spraying removes dirt from the wafers, after they are pulled through the surface.
**Ultrasonic/Megasonic Cleaning**

Ultrasonic -> 20-50kHz -> Cavities in Water (Bubbles)
Megasonic -> 850 kHz -> Mobilizes Surface Hydration Layer
### Evolution of DI water specifications

<table>
<thead>
<tr>
<th></th>
<th>Process technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>256K DRAM</td>
</tr>
<tr>
<td>Design rule, μm</td>
<td>2.0</td>
</tr>
<tr>
<td>Resistivity, MΩ-cm</td>
<td>&gt; 17.0</td>
</tr>
<tr>
<td>Particle (pieces/cc)</td>
<td>-</td>
</tr>
<tr>
<td>&gt; 0.2 μm</td>
<td>&lt; 30</td>
</tr>
<tr>
<td>&gt; 0.1 μm</td>
<td>&lt; 50</td>
</tr>
<tr>
<td>&gt; 0.085 μm</td>
<td></td>
</tr>
<tr>
<td>&gt; 0.05 μm</td>
<td></td>
</tr>
<tr>
<td>Bacteria, unit/L</td>
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</tr>
<tr>
<td>TOC, ppb</td>
<td>&lt; 100</td>
</tr>
<tr>
<td>Oxygen, ppb</td>
<td>&lt; 100</td>
</tr>
<tr>
<td>Silica, ppb</td>
<td>&lt; 10</td>
</tr>
<tr>
<td>Na, ppb</td>
<td>1</td>
</tr>
<tr>
<td>Cl, ppb</td>
<td>1</td>
</tr>
<tr>
<td>Metal ion, ppb</td>
<td>1</td>
</tr>
</tbody>
</table>

*Source:* Courtesy of Christ AG, Switzerland.
**Mind the amount!**

Environment, Safety, and Health

![Graph showing UPW usage](image)

**Figure 7** Ultrapure water (UPW) per square inch of silicon used in wafer processing at 16 U.S. fabs. UPW usage is plotted versus wafer size and the number of masks levels. (From Ref. 14.)

**Table 2** Production statistics averaged over ten largest fabs at each wafer size. Wafer starts for 300 mm are estimated by simple extrapolation from smaller wafer sizes.

<table>
<thead>
<tr>
<th>Wafer Diameter (mm)</th>
<th>Wafer Starts per Month</th>
<th>in²/year (Millions)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>38300</td>
<td>5.6</td>
</tr>
<tr>
<td>150</td>
<td>32500</td>
<td>10.7</td>
</tr>
<tr>
<td>200</td>
<td>27600</td>
<td>16.1</td>
</tr>
<tr>
<td>300</td>
<td>22074</td>
<td>29.0</td>
</tr>
</tbody>
</table>

Source: Dataquest (Ref. 3).
Ultra-pure bulk gas purity requirements

<table>
<thead>
<tr>
<th>Limits for 300 mm</th>
<th>Nitrogen</th>
<th>Hydrogen</th>
<th>Oxygen</th>
<th>Argon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Water</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
</tr>
<tr>
<td>Oxygen</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>100%</td>
<td>&lt;100 ppt</td>
</tr>
<tr>
<td>Carbon</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
</tr>
<tr>
<td>Sulfur</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
</tr>
<tr>
<td>Nitrogen</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
<td>&lt;100 ppt</td>
</tr>
<tr>
<td>Particles\textless\textgreater\mu m</td>
<td>&gt;0.1</td>
<td>&lt;0.1</td>
<td>&lt;0.1</td>
<td>&lt;0.1</td>
</tr>
</tbody>
</table>

Table 18 Specialty gas quality requirements

<table>
<thead>
<tr>
<th>Typical Limits for 300 mm</th>
<th>Corrosives/toxics</th>
<th>Pyrophorics</th>
<th>Inerts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contaminant</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Water</td>
<td>&lt;500 ppbv</td>
<td>NA</td>
<td>&lt;500 ppbv</td>
</tr>
<tr>
<td>Oxygen</td>
<td>&lt;100 ppbv</td>
<td>NA</td>
<td>&lt;1000 ppbv</td>
</tr>
<tr>
<td>Metallics</td>
<td>&lt;100 pptwt</td>
<td>&lt;100 pptwt</td>
<td>&lt;100 pptwt</td>
</tr>
<tr>
<td>Particles</td>
<td>&lt;2/liter</td>
<td>&lt;2/liter</td>
<td>&lt;2/liter</td>
</tr>
</tbody>
</table>
**Clean Design Consideration**

**Table 14  Clean-room specifications**

<table>
<thead>
<tr>
<th>Typical 300 mm requirements</th>
<th>Target</th>
<th>Limits</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vibration</td>
<td>&lt;125 μ-inch/sec</td>
<td>3–30 Hz</td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>NC 50</td>
<td>&lt;NC55</td>
<td></td>
</tr>
<tr>
<td>Lighting</td>
<td>80 FC white</td>
<td>±5 FC</td>
<td></td>
</tr>
<tr>
<td>Conductivity</td>
<td>10$^7$ ohms/sq.</td>
<td>10$^3$–10$^9$</td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td>70°F</td>
<td>68°F–72°F</td>
<td></td>
</tr>
<tr>
<td>Humidity</td>
<td>44%</td>
<td>44%–48%</td>
<td></td>
</tr>
<tr>
<td>Pressure</td>
<td>0.06 WC</td>
<td>±0.01 WC</td>
<td></td>
</tr>
<tr>
<td>Particles</td>
<td>0.05 WC</td>
<td>±0.01 WC</td>
<td></td>
</tr>
<tr>
<td>Airborne contaminants/aerosols</td>
<td>all &gt;0.1 μm</td>
<td>&lt;35/M$^3$</td>
<td>Maintain positive pressure</td>
</tr>
<tr>
<td></td>
<td>all &gt;0.06 μm</td>
<td>&lt;5/M$^3$</td>
<td></td>
</tr>
<tr>
<td>Laminar velocity</td>
<td>80 fpm</td>
<td>70–90 fpm</td>
<td></td>
</tr>
<tr>
<td>Ceiling coverage in photo</td>
<td>50%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ceiling coverage outside photo</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Organics: <100 pptM, Amines: <1000 pptM, Metals: <0.2 pptM, Acids: <10 pptM, Bases: <20 pptM, As MW=250 E=10$^5$, As Cu, E=2×10$^5$, As Cl−, E=10$^5$, As Na+, E=10$^6$, May be turbulent for SMIF.*
Oxidation Layering.

Oxidation layering produces a thin layer of silicon dioxide, or oxide, on the substrate by exposing the wafer to a mixture of high-purity oxygen or water at ca. 1000°C (1800°F).