Text Book:
Silicon VLSI Technology
Fundamentals, Practice and
Modeling
Authors: J. D. Plummer, M. D. Deal,
and P. B. Griffin
Crystal Growth, Wafer Fab and Properties

• High Quality Single Crystal Wafers

• Diameter
• Thickness
• Flatness
• Mechanical defects (scratches)
• Crystallographic Defects (dislocation density)
• Crystal Orientation
• Impurity Level
• Dopant Type and Density-Resistivity
Silicon Structure Classification

- Single Crystal – periodic arrangement of atoms
- Polycrystalline – small crystals of arbitrary alignment
- Amorphous Silicon – no significant ordering of atoms

- Simple Crystal Unit Cells
  - Cubic
  - Body-Centered Cubic (extra atom in the body)
  - Face-Centered Cubic (extra atoms centered on faces)
Crystal Planes

- Planes and directions are defined using an x, y, z coordinate system.
  - [111] direction is defined by a vector having components of 1 unit in x, y and z.
- Planes are defined by Miller indices
  - Defined as the reciprocals of the intercepts of the plane with the x, y and z axes.
Silicon Lattice

- Diamond cubic lattice
  - Two merged FCC lattices with the origin of the second offset from the first by a/4 in all three directions
  - Covalent bonding to four nearest neighbors

Figure 3-3 Diamond crystal structure of silicon. The unit cell may be visualized as two merged FCC cells, offset from each other by a/4 in all three directions. (a) shows the basic FCC unit cell. (b) shows two merged cells, offset by a/4. In (c), with the four atoms in the second FCC cell that lie within the first FCC cell are shown. The arrows show the corresponding a/4 displacement of these four atoms. In (d), the actual tetragonal bonding between the atoms in the diamond cell is shown.
Semiconductor Lattices

- 3D Model of unit cells for semiconductors
  http://jas.eng.buffalo.edu/education/solid/unitCell/home.html
  - from: http://jas.eng.buffalo.edu/index.html
  multiple semiconductor applets
Si licon Surface Plane Differences

- Bulk properties are generally isotropic with the symmetric lattice
- Dopant diffusion is independent as long as surfaces play no role in the process.
  - However, real devices are built near surfaces.
  - The plane that the surface terminates on can then make a difference.
  - [111] has the highest number of atoms per cm$^2$ \( \frac{1}{B} \times 4 \times \frac{1}{2} \times 1 = 1 \)
  - [100] has the lowest (dominant type used)
- Concerns:
  - Oxidation rates, surface defect density, "near" surface diffusion
Defects in Crystals

- Various types of defects can exist in crystal (or can be created by processing steps. In general these are detrimental to device performance.

- Linear Defects: Dislocation due to high stress or rapid thermal gradients
- Volume Defects: Agglomeration of point defects Precipitate of dopants

Point Defects:
- V missing/vacancy
- I extra atom/interstitial
Stacking Fault

- Form along the \{111\} plane
  - The insertion or removal of an extra \{111\} plane
  - Normally referred to as ABCABC...
  - Extrinsic adds a plane ABCACBC... (excess interstitials)
    - Dominant type
    - Oxidation Induced Stacking Faults
  - Intrinsic if a plane is missing ABCABABC...
Raw Material and Purification

- Raw Material – Quartzite SiO₂
- Convert Quartzite into metallurgical grade silicon or (MGS)
  - Furnace with quartzite and carbon (coal or coke) @ 2000 °C
  - ~ 98% pure
  \[ 2C(solid) + SiO₂(solid) \rightarrow Si(liquid) + 2CO \]
- MFGS converted to electronics grade silicon (EGS)
  - MGS powder combined with gaseous HCl
  - Produce SiH₄ (silane), SiH₅Cl (chlorosilane), SiH₃Cl₂ (dichlorosilane), SiHCl₃ (trichlorosilane), or SiCl₄ (silicon tetrachloride)
Raw Material and Purification (2)

- SiHCl$_3$ (trichlorosilane) processing
  - Room temperature liquid that can be purified using fractional distillation. Boiled and condensed back into a liquid.

- Chemical vapor deposition
  - SiHCl$_3$ (gas) and hydrogen (gas) with Si rod
    \[ 2\text{SiHCl}_3(\text{gas}) + 2\text{H}_2(\text{gas}) \rightarrow 2\text{Si(solid)} + 6\text{HCl(gas)} \]
  - Deposition of polysilicon (parts per billion purity)
    \[ 10^{13} \text{ to } 10^{14} \text{ cm}^{-3} \text{ impurities} \]

- Polysilicon used for either:
  - Czochralski (CZ) crystal growth
  - Float-Zone (FZ) crystal growth
Crystal Growth

• The raw material contains < 1 ppb impurities. Pulled crystals contain O ($\approx 10^{18} \text{ cm}^{-3}$) and C ($\approx 10^{16} \text{ cm}^{-3}$), plus any added dopants placed in the melt.

• Essentially all Si wafers used for ICs today come from Czochralski (cho-HRAL-skee) grown crystals.

• Polysilicon material is melted, held at close to 1417 °C, and a single crystal seed is used to start the growth.

• Pull rate, melt temperature and rotation rate are all important control parameters.

• Approximately $50 per 8 \text{ in.} wafer when text written
Crystal Growth (2)

(More information on crystal growth at http://www.memc.com)

(Photo courtesy of Ruth Carranza)

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Float Zone Crystal Growth

- An alternative process is the float zone process which can be used for refining or single crystal growth.
- Localized $I^2R$ heating via RF Coil
  - Nitrogen or dopant ambient
- Wafers < 150 mm
  - Detectors and power
  - Doping is a challenge
  - Reduced C and O impurities
- Bottom in contact with single crystal seed
Silicon Wafer Diameter

![Silicon Wafer Diameter History and Forecast](image)


Ingot Cutting into Wafers

After crystal pulling, the boule is shaped and cut into wafers which are then polished on one side.

(See animations of crystal polishing etc. at http://www.mcmc.com)
**Wafer Preparation and Specification**

Mark wafer earlier (laser process) to track their process flow

- Grind crystal to a diameter (200mm<=750μm) ... 850μm thick
- Grind flats (the primary and secondary)
- Saw of the boule into wafers
- Lapping, etching (batch process in acids etching Si) 20μm, polishing (chemical-mechanical) 25μm removes damage and improves flatness ±2μm

Suspension

Al₂O₃

SiO₂ 10nm in NaOH/DI

**CMP**

3Si +4HNO₃+18HF ⇌3H₂SiF₆+4NO+8H₂O

**Figure 3-8** The upper figures were taken directly from the Silicon Database on the Mitsubishi Materials Silicon Corporation web site at www.egg.or.jp/MSIL/english/index-e.html. They conceptually illustrate the wafer polishing operation. An actual machine is shown below. Photo courtesy of R. Carranza.
MEMC Process Animation

- Crystal Pulling
- Rod Grinding
  - Achieving the correct diameter
  - Grinding flats for crystal orientation
- Wire Cutting
  - 100 mm, 150 mm, 200 mm, 300 mm, 450 mm
- Edge Profiling
- Lapping
  - Improve wafer flatness
- Etching and Polishing
- Laser Inspection
Measurement Methods

- Sheet Resistance
  - Co-linear four-point probe
  - Van der Pauw
- Hot Point Probe
- Hall Effect
**Measurements of the Grown Crystal**

Resistivity \[ \rho = \frac{1}{q\mu_n + q\mu_p} \text{[\(\Omega \text{cm}\)]} \]

![Diagram of four-point probe method](image)

\[ V = \frac{\rho I}{2\pi r} \]

\[ \rho = \frac{V}{2\pi r I} \text{[\(\Omega \text{cm}\)]} \]

\[ x_j << t \]

\[ \Phi >> s \]

**Average resistivity** \[ \rho = \frac{\pi t}{\ln(2)} \frac{V}{I} = 4.532 \frac{V}{I} x_j \text{[\(\Omega \text{cm}\)]} \]

**Sheet resistance** \[ \rho_s = \frac{b}{x_j} \frac{\pi}{\ln(2)} \frac{V}{I} = 4.532 \frac{V}{I} \text{[\(\Omega \text{/square}\)]} \]
Measurements of the Grown Crystal

Conductivity Type

Seebeck voltage

Electrons move - Donors stay
N Type
Si Wafer

25-100°C hotter

Electron current

\[ J_n = qn \mu_n F_n \frac{dT}{dx} \]

Sign of the voltage V tells what is the conductivity type
**Hall Effect Measurement**

Measurements of majority carrier concentrations (and type) and their mobility \( \overline{J_x} \) w/o B field

![Test structure diagram]

Electrons at the bottom

**Figure 3-13** Conceptual representation of Hall effect measurement. The right sketch is a top view of a more practical implementation.

- Force: \( Q(\varepsilon + v \times B) \)
- \( F_y = q(\varepsilon_r + v_x B_x) = 0 \)
- \( \varepsilon_y = -B_x v_x = B_x \frac{J_x}{q\sigma} \)
- \( V_y = B_x \frac{J_x}{q\sigma} \)
- \( R_H = \frac{V_y}{B_x J_x} \)
- \( \rho, n = \pm \frac{1}{qR_H} \)
- \( v_H = \frac{|R_H|}{\rho} = |R_H|\sigma \)
Measuring Impurities

Fourier Transport Infrared Spectroscopy (FTIR)

For Interstitial Oxygen incorporated during CZ growth and Substitutional Carbon (detection limit O- $2 \times 10^{15} \text{cm}^{-3}$, C- $5 \times 10^{15} \text{cm}^{-3}$)

Sweep the wavelength of incident energy → look for absorption

detection of absorbed wavelengths

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SEM and TEM

• Scanning Electron Microscope
  – Large depth of focus
  – Magnification 300,000x
  – Resolution below 5 nm

• Transmission Electron Microscope
  – Prepared samples
    (1 um thickness)
  – Resolution is about 0.2 nm

Figure 3-15 TEM image of the Si/SiO₂ interface. The crystalline structure of the silicon is visible on the bottom. The thermally grown SiO₂ is amorphous. Photo courtesy of John Bravman, Stanford University.
Models and Simulation

- Czochralski Crystal Growth
- Dopant Incorporation in CZ
- Zone Refining and FZ Growth
- Point Defects
- Oxygen in Silicon
- Carbon in Silicon
Modeling Crystal Growth

- We wish to find a relationship between pull rate and crystal diameter.
- Freezing occurs between isotherms $X_1$ and $X_2$.
- Heat balance:
  - latent heat of crystallization + heat conducted from melt to crystal = heat conducted away.

\[ L \frac{dm}{dt} + k_L \frac{dT}{dx_1} A_1 = k_s \frac{dT}{dx_2} A_2 \]

$L$ = latent heat of fusion
\[ \frac{dm}{dt} \] = amount of freezing per unit time
$k_L$ = thermal conductivity of liquid
\[ \frac{dT}{dx_1} \] = thermal gradient at isotherm $x_1$
$k_s$ = thermal conductivity of solid
\[ \frac{dT}{dx_2} \] = thermal gradient at $x_2$
Model Crystal Growth (2)

- The rate of growth of the crystal is where $v_p$ is the pull rate and $N$ is the density and $A$ the cross sectional area.

- Neglecting the middle term in Eqn. (1) we have:

\[
\frac{dm}{dt} = v_p \cdot A \cdot N \quad (2)
\]

\[
L \frac{dm}{dt} \leq k_s \frac{dT}{dx_2} A_2
\]

\[
v_p \cdot A \cdot N \cdot L \leq k_s \frac{dT}{dx_2} A_2
\]

\[
V_{\text{MAX}} = \frac{k_s}{L} \frac{dT}{dx_2} \quad (3)
\]
Model Crystal Growth (3)

- In order to replace $dT/dx$, we need to consider the heat transfer processes.
- Latent heat of crystallization (A) transfers up the crystal (B) and is lost by radiation (C).

- Heat radiation from the crystal (C) is given by the Stefan-Boltzmann law
  \[ dQ = (2\pi rd^3) \cdot (\sigma \varepsilon T^4) \]  \[ (4) \]

- Heat conduction up the crystal is given by
  \[ Q = k_s \left( \pi \cdot r^2 \right) \cdot \frac{dT}{dx} \]  \[ (5) \]

- Differentiating (5), we have
  \[ \frac{dQ}{dx} = k_s \left( \pi r^2 \right) \frac{dT}{dx} + \left( \pi r^2 \right) \frac{d^2T}{dx^2} \frac{dk_s}{dx} \approx k_s \left( \pi r^2 \right) \frac{d^2T}{dx^2} \]  \[ (6) \]
Model Crystal Growth (4)

- Substituting (6) into (4), we have

\[ \frac{d^2T}{dx^2} - \frac{2\sigma e}{k_s r} T^4 = 0 \]  \hspace{1cm} (7)

- \( k_s \) varies roughly as 1/T, so if \( k_M \) is the thermal conductivity at the melting point,

\[ k_s = k_M \frac{T_M}{T} \]  \hspace{1cm} (8)

\[ \therefore \frac{d^2T}{dx^2} - \frac{2\sigma e}{k_M r T_M} T^4 = 0 \]  \hspace{1cm} (9)

- Solving this differential equation, evaluating it at \( x = 0 \) and substituting the result into (3), we obtain

\[ T = \left( \frac{3k_M r T_M}{8\sigma e} \right)^{\frac{1}{4}} \left( x + \left( \frac{3k_M r}{8\sigma e T_M^3} \right)^{\frac{1}{2}} \right)^{\frac{1}{2}} \]  \hspace{1cm} (10)

\[ v_{\text{MAX}} = \frac{1}{L N} \sqrt{\frac{2\sigma k_M T_M^3}{3r}} \]

- Using the example on p. 124, this gives a max pull rate of \( \approx 24 \text{ cm hr}^{-1} \) for a 6” crystal (Actual values are \( \approx 2X \) less than this).
Monitoring Ingot Growth

- Automation of the process incorporates numerous sensors and feedback
  - Optical monitoring of resulting crystal diameter
  - Infrared sensing of temperature
  - Thermocouples for specific temperatures within chamber
Modeling Dopant Behavior During Crystal Growth

- Dopants are added to the melt to provide a controlled N or P doping level in the ingot and resulting wafers.
  - The dopant incorporation process is complicated by dopant segregation, a difference in the impurity concentration between the liquid and solid.
  - Segregation occurs between the liquid and solid phase of material when they are in intimate contact. An experimentally measured segregation coefficient defines the difference between the two.

\[ k_o = \frac{C_s}{C_L} \]
Segregation Coefficient

<table>
<thead>
<tr>
<th>Dopant</th>
<th>$k_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>As</td>
<td>0.3</td>
</tr>
<tr>
<td>Bi</td>
<td>$7 \times 10^{-4}$</td>
</tr>
<tr>
<td>C</td>
<td>0.07</td>
</tr>
<tr>
<td>Li</td>
<td>$10^{-2}$</td>
</tr>
<tr>
<td>O</td>
<td>0.5</td>
</tr>
<tr>
<td>P</td>
<td>0.35</td>
</tr>
<tr>
<td>Sb</td>
<td>0.023</td>
</tr>
<tr>
<td>Al</td>
<td>$2.8 \times 10^{-3}$</td>
</tr>
<tr>
<td>Ga</td>
<td>$8 \times 10^{-3}$</td>
</tr>
<tr>
<td>B</td>
<td>0.8</td>
</tr>
<tr>
<td>Au</td>
<td>$2.5 \times 10^{-5}$</td>
</tr>
</tbody>
</table>

$k_0 = \frac{C_S}{C_L}$

- Most $k_0$ values are $<1$; therefore, the impurity prefers to stay in the liquid.
- Thus as the crystal is pulled $C_L$ increases.
- As the melt concentration increases, the silicon crystal doping, $N_{Si}$, will also increase.
Dopant Model

- If during growth, an additional volume $dV$ freezes, the impurities $(I)$ incorporated into the volume $dV$ are given by

$$dl = -k_0 C_L dV = -k_0 \frac{I_L}{V_o - V_S} \cdot dV$$  \hspace{1cm} (12)

$$\int_{I_0}^{I_L} \frac{I}{I_0} \cdot \frac{dV}{V_o - V_S} = \int_{I_0}^{I_L} I \cdot dV$$  \hspace{1cm} (13)

$$\log \left( \frac{I_L}{I_0} \right) = -k_0 \cdot \log \left( \frac{V_o}{V_o - V_S} \right)$$

$$I_L = I_0 \left( 1 - \frac{V_o}{V_o} \right)^{-k_0}$$  \hspace{1cm} (14)

- This equations defines the number of impurities in the melt as a function of how much of the melt has solidified.
Dopant Model (2)

- Knowing the number of impurities in the melt as a function of how much of the melt has solidified. We define the fraction of melt “frozen” as $f$.

\[
f = \frac{V_s}{V_0}
\]

\[
I_L = I_o (1 - f)^{k_o}
\]

- The impurities in the crystal ($C_S$) can then be computed using

\[
C_s \propto \frac{dI_L}{dV_s} \tag{15}
\]

\[
C_s = C_o k_o (1 - f)^{o - 1} \tag{16}
\]

- This equations defines expected impurity concentration in the resulting wafers based on their location in the crystal. This is directly related to the amount of melt solidified in the ingot pulling process, $f=0$ to $f=1$. 
Doping Concentration vs. Position

- Plot of Eq. (16).
- Note the relatively flat profile produced by boron with a $k_S$ close to 1.
- Dopants with $k_S \ll 1$ produce much more variation in doping concentration along the crystal.
Float Zone Growth and Refining

- In the float zone process, dopants and other impurities tend to stay in the liquid; therefore, refining can be accomplished, especially with multiple passes.

- See the text for models of this process.

\[
C_3(x) = C_0 \left( 1 - (1 - k_o) \cdot e^{\frac{k_o \cdot x}{L}} \right)
\]
FZ Impurity Behavior

Figure 3-20 Behavior of impurities during float-zone growth or zone refining. The solid is counted to start with a uniform doping concentration $C_0$. The curves correspond to one pass of the solid zone through the solid.

Figure 3-21 Zone refining with multiple passes. $C_0 = 0.1$ in this example.
Modeling Point Defects

- Vacancies (V) and Interstitials (I)
- The existence of defects minimizes the total free energy of the crystal. Therefore, they will exist for all temperatures above absolute zero.
  - The concentrations can be related as

\[ C_V^*, C_I^* = N_S \exp \left( \frac{S_f^*}{k} \right) \exp \left( -\frac{H_f^*}{kT} \right) \]

- \( S_f^* \) is the formation entropy of the defect
- \( H_f^* \) is the enthalpy of formation of the defect
- \( N_S \) is the number density of lattice sites
- * denotes equilibrium
Point Defect Equilibrium

- The Frenkel process: moving a silicon atom off from a lattice site inside a crystal. It creates equal number of V and I.
- I created if silicon atom moves from the surface into the bulk.
- V and I can be recombined removing one of each
- Stacking fault can capture either V or I by growing or shrinking but one lattice site
- In general, there is an assumption that the equilibrium population rate of change is due to kinematics and is assumed to change “immediately” with respect to temperature.
  - With the exception of ion implantation and CZ growth

- Estimated values for Silicon

\[
C_{v0}^* \approx 1 \times 10^{27} \exp \left( \frac{-3.8eV}{kT} \right) \\
C_{i0}^* \approx 9 \times 10^{23} \exp \left( \frac{-2.6eV}{kT} \right)
\]
Concentration Example

- At 1000 °C

\[ k \approx 8.617343 \times 10^{-5} \text{ cm}^{-3} \]

\[ C_{j^0}^* \approx 1 \times 10^{12} \text{ cm}^{-3} \]

\[ C_{p^0}^* \approx 5 \times 10^{12} \text{ cm}^{-3} \]

\[ n_i \approx 7.14 \times 10^{18} \text{ cm}^{-3} \]

\[ N_D, N_A \approx 10^{15} \text{ to } 10^{20} \text{ cm}^{-3} \]

Defects are present but a concentrations significantly less than carriers and difficult to detect.
Point Defect Diffusivities

- Point defects are extremely mobile.
  - Crystal kinematics.
  - Not directly measured, but has been inferred from dopant diffusivity.

\[
d_i \approx 51 \exp \left( \frac{-1.8eV}{kT} \right) \text{cm}^2 \cdot \text{sec}^{-1}
\]

\[
d_v \approx 3.65 \times 10^{-4} \cdot \exp \left( \frac{-1.58eV}{kT} \right) \text{cm}^2 \cdot \text{sec}^{-1}
\]
Modeling Point Defects in Silicon

- Point defects (V and I) will turn out to play fundamental roles in many process technologies.
- The total free energy of the crystal is minimized when finite concentrations of these defects exist.

![Image of crystal structure with point defects](image)

- In general $C_{V^0} \neq C_{I^0}$ and both are strong functions of temperature.
- Kinetics may determine the concentration in a wafer rather than thermodynamics.
Charged Point Defects

• Shockley and Last (1957) first described these charged defect concentrations.

• V and I also exist in charged states with discrete energies in the Si bandgap.
  – In N type Si, V⁻ and V will dominate
  – In P type, V⁺ and V''⁺ will dominate.

<table>
<thead>
<tr>
<th>EF for an N type material</th>
<th>EC</th>
<th>VA</th>
<th>VB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Table 3-3: Estimated energy levels of Fermi / energy levels in the silicon bandgap. |
|---------------------------------|--------------|--------------|--------------|
|                                | EC - EF     | EC - EF     | EC - EF     |
| EF - VA                        | 0.57 eV     | 0.3 eV ??    | ??           |
| EF - VB                        | 0.11 eV     | 0.2 eV ??    | ??           |
| EF - VB                        | 0.05 eV     | 0.4 eV ??    | ??           |
| EF - V                         | 0.33 eV     | 0.0 eV ??    | ??           |
| EF - V                         | 0.33 eV     | 0.0 eV ??    | ??           |
Charged Point Defects

• For intrinsic silicon, no change in charge occupation
• For extrinsic N type Si, \( V^- \) and \( V^- \) will dominate as the Fermi energy rises
  – The dominant vacancy charge state becomes \( V^- \) acting like an acceptor
• For extrinsic P type Si, \( V^+ \) and \( V^{++} \) will dominate. As the Fermi energy falls
  – The dominant vacancy charge state becomes \( V^+ \) acting like a donor

\[ \begin{array}{c}
E_C \\
V^- \\
V^+ \\
E_V \\
E_F \text{ for an N type material}
\end{array} \]

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Charge Defect Concentrations

\[ C_{V^+}^* = C_{V^0}^* \exp\left(\frac{E_{V^+} - E_F}{kT}\right) \]

\[ C_{V^-}^* = C_{V^0}^* \exp\left(\frac{E_F - E_{V^-}}{kT}\right) \]

- Shockley and Last (1957) first described these charged defect concentrations (see text).

Note:
- The defect concentrations are always \( < n_c \) (doping \( \rightarrow \) \( E_F \rightarrow \) point defect concentrations)
- As doping changes, the neutral point defect concentrations are constant.
- However, the charged defect concentrations change with doping.

\( \therefore \) the total point defect concentrations change with doping.
Point Defect Example

- At 1000 °C, the P region will be intrinsic, the N region is extrinsic.
- $E_g \sim 0.7778$ eV
- Compute $n_i$ and check $N_D$ and $N_A$
- Construct energy band diagram

Intrinsic: Fermi Level in middle

Figure 3.24 Calculated bandgap, point defect energy levels and Fermi levels at 1000°C.
Point Defect Example

\[
\begin{array}{c}
N: 5 \times 10^{19} \text{ cm}^{-3} \\
P: 10^{15} \text{ cm}^{-3}
\end{array}
\]

- Compute \( V^0 \) and \( I^0 \)
- Compute P-type \( V \) and \( I \)

<table>
<thead>
<tr>
<th>Doping</th>
<th>P Region</th>
<th>N Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>( n_i )</td>
<td>( 7.14 \times 10^{18} \text{ cm}^{-3} )</td>
<td>( 7.14 \times 10^{18} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( V^0 )</td>
<td>( 4.6 \times 10^{13} \text{ cm}^{-3} )</td>
<td>( 4.6 \times 10^{13} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( V^- )</td>
<td>( 2.37 \times 10^{14} \text{ cm}^{-3} )</td>
<td>( 1.61 \times 10^{15} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( V^+ )</td>
<td>( 1.85 \times 10^{13} \text{ cm}^{-3} )</td>
<td>( 8.50 \times 10^{14} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( V^{++} )</td>
<td>( 2.08 \times 10^{12} \text{ cm}^{-3} )</td>
<td>( 3.06 \times 10^{11} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( I^0 )</td>
<td>( 1.94 \times 10^{11} \text{ cm}^{-3} )</td>
<td>( 4.23 \times 10^9 \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( I^- )</td>
<td>( 9.13 \times 10^{11} \text{ cm}^{-3} )</td>
<td>( 9.13 \times 10^{11} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( I^+ )</td>
<td>( 4.02 \times 10^{11} \text{ cm}^{-3} )</td>
<td>( 2.73 \times 10^{12} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>( I^{++} )</td>
<td>( 8.32 \times 10^{10} \text{ cm}^{-3} )</td>
<td>( 1.48 \times 10^{11} \text{ cm}^{-3} )</td>
</tr>
</tbody>
</table>

**Note:**
- \( n_i \) relative to doping in the two regions.
- \( V^0 \) is the same in the two regions.
- Different charge states dominate in the different regions.
Oxygen and Carbon in CZ Silicon

- The CZ growth process inherently introduces O and C.
- Typically, $C_O \approx 10^{18}$ cm$^{-3}$ and $C_C \approx 10^{18}$ cm$^{-3}$.
- The O in CZ silicon often forms small SiO$_2$ precipitates in the Si crystal under normal processing conditions.

- O and these precipitates can actually be very useful.
  - Provide mechanical strength.
  - Internal gettering (described later in Chapter 4).
Summary of Key Ideas

- Raw materials (SiO2) are refined to produce electronic grade silicon with a purity unmatched by any other commonly available material on earth.
- CZ crystal growth produces structurally perfect Si single crystals which can then be cut into wafers and polished as the starting material for IC manufacturing.
- Starting wafers contain only dopants, O, and C in measurable quantities.
- Dopant incorporation during crystal growth is straightforward except for segregation effects which cause spatial variations in the dopant concentrations.
- Point, line, and volume (1D, 2D, and 3D) defects can be present in crystals, particularly after high temperature processing.
- Point defects are "fundamental" and their concentration depends on temperature (exponentially), on doping level and on other processes like ion implantation which can create non-equilibrium transient concentrations of these defects.
Semiconductor Electronics:
Silicon

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Preparation of Silicon

• In the following, we will look at how wafers are made.
• There are very few and very specialized companies that make wafers
• Generally, you will buy wafers to start your process.
Purity!

High Purity Sand (Quartzite)
\[ \text{SiO}_2 + \text{C} \text{ (coal, coke, wood)} \rightarrow \]
\[ \text{Si} + \text{SiO} \text{ (gas)} + \text{CO} \text{ (gas)} \]

Polycrystalline Silicon, 
Metallurgical Grade (98%)
Purity!

Polycrystalline Silicon, Metallurgical Grade (98%)

$\text{Si} + \text{HCl (gas)} \rightarrow \text{SiCl}_3\text{H} + \text{H}_2$

Trichlorosilane (liquid at RT, bp=32C) Fractional distillation increases purity to ppb level
Purity!

Trichlorosilane (liquid at RT, bp=32C)

\[ \text{SiCl}_3 \text{H} + \text{H}_2 \rightarrow \text{Si} + 3 \text{HCl} \]

Thermal decomposition on hot filaments yields Electronics Grade Silicon (ppb level impurity)
Semiconductor Processing: Overview.

Si + HF(aqu.), precipitation in ingots

Polycrystalline silicon tubes are dissolving in hydrofluoric acid to produce polysilicon ingots.

Because polycrystalline silicon has randomly oriented crystallites, it doesn't have the electrical characteristics necessary for semiconductor device fabrication. It must first be transformed into single crystal silicon using a process called Crystal Pulling.
Single crystal silicon ingots are produced with a crystal pulling process called the CZ (Czochralski) method.

Crushed high-purity polycrystalline silicon + dopands (e.g. boron or phosphorous) and melted at 1400° in a quartz crucible surrounded by an inert gas atmosphere of high-purity argon. The melt is cooled to a precise temperature, then a "seed" of single crystal silicon is placed into the melt and slowly rotated as it is "pulled" out.
The surface tension between the seed and the molten silicon causes a small amount of the liquid to rise with the seed and cool into a single crystalline ingot with the same orientation as the seed.

The ingot diameter is determined by a combination of temperature and extraction speed.

Most ingots produced today are 150mm (6") and 200mm (8") diameter, but the industry is also using 300mm (12") and 400mm (16") ingots.
Dopants

TABLE 2.1 Equilibrium Segregation Coefficients for Dopants in Silicon

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<th>Dopant</th>
<th>$k_0$</th>
<th>Type</th>
<th>Dopant</th>
<th>$k_0$</th>
<th>Type</th>
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<td>B</td>
<td>$8 \times 10^{-1}$</td>
<td>p</td>
<td>As</td>
<td>$3.0 \times 10^{-1}$</td>
<td>n</td>
</tr>
<tr>
<td>Al</td>
<td>$2 \times 10^{-3}$</td>
<td>p</td>
<td>Sb</td>
<td>$2.3 \times 10^{-2}$</td>
<td>n</td>
</tr>
<tr>
<td>Ga</td>
<td>$8 \times 10^{-3}$</td>
<td>p</td>
<td>Te</td>
<td>$2.0 \times 10^{-4}$</td>
<td>n</td>
</tr>
<tr>
<td>In</td>
<td>$4 \times 10^{-4}$</td>
<td>p</td>
<td>Li</td>
<td>$1.0 \times 10^{-2}$</td>
<td>n</td>
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<tr>
<td>O</td>
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<td>Cu</td>
<td>$4.0 \times 10^{-4}$</td>
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<td>C</td>
<td>$7 \times 10^{-2}$</td>
<td>n</td>
<td>Au</td>
<td>$2.5 \times 10^{-3}$</td>
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<td>P</td>
<td>0.35</td>
<td>n</td>
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*Deep-lying impurity level.

- Typically B, P, As, Sb
- Dopant Concentration in melt different than in precipitate
- Problem: If $k_0$ is not 1, then the concentration in the melt changes and hence along the length of the rod
- Dopant concentration in melt is increasing

$K_0 = \frac{C_s}{C_l}$
Doping Gradient

Figure 2.4 Curves for growth from the melt showing the doping concentration in a solid as a function of the fraction solidified.†
Float Zone Crystal Growth

- Speciality Process
- Higher Purity
- Lower Charge Carrier Density
- More Dislocation
- High-Voltage Applications
- More Expensive
Dopants Stay in the Melt

Dopants prefer to be in the Melt
Multiple Float Zone Passes can purify material
Initial extremely high dopant concentration travel with the melt and produce rather uniform dopant concentration
## CZ vs. Float Zone

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<th>CZ</th>
<th>FLOAT ZONE</th>
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<td>Cost</td>
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<td>Dislocations</td>
<td>$0 - 10^4/cm^2$</td>
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<td>Resistivity</td>
<td>Up to 100 ohm·cm</td>
<td>2000 ohm·cm Max.</td>
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<td>Radial</td>
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<tr>
<td>Resistivity</td>
<td>5 - 10%</td>
<td>5 - 10%</td>
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<tr>
<td>Oxygen Content</td>
<td>$10^{16} - 10^{18}$ atoms/cm$^3$</td>
<td>0 - Very Low</td>
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### TABLE 2.4 Comparison of Silicon Material Characteristics and Requirements for ULSI

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<tr>
<th>Property</th>
<th>Characteristics</th>
<th>Czochralski</th>
<th>Float Zone</th>
<th>Requirements for ULSI</th>
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<td>Resistivity (phosphorus) n-type (ohm-cm)</td>
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<td>1–50</td>
<td>1–300 and up</td>
<td>5–50 and up</td>
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<td>Resistivity (antimony) n-type (ohm-cm)</td>
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<td>0.005–10</td>
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<td>0.001–0.02</td>
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<td>Resistivity (boron) p-type (ohm-cm)</td>
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<td>0.005–50</td>
<td>1–300</td>
<td>5–50 and up</td>
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<td>Resistivity gradient (four-point probe) (%)</td>
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<td>Minority carrier lifetime (μs)</td>
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<td>30–300</td>
<td>50–500</td>
<td>300–1000</td>
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<td>Not detected</td>
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<td>≤ 1</td>
<td>≤ 0.01</td>
<td>&lt; 0.001</td>
</tr>
</tbody>
</table>

ppma, parts per million atoms, ppba, parts per billion atoms.
Resistivity Profile

Figure 2.9  (a) Typical lateral resistivity distribution in a conventionally doped silicon. (b) Silicon doped by neutron irradiation.5

Page 16
End Cropping

Removal of the conical parts at top and bottom of the ingot
Wafer Size Considerations

Figure 6.5 Effect of larger wafer diameter on percentage of partial die.

Figure 6.6 Effect of processing larger die on larger wafers.
### Wafer Size Considerations

<table>
<thead>
<tr>
<th>Die Size (mils)</th>
<th>Wafer Diameter (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>100</td>
</tr>
<tr>
<td>200x200</td>
<td>283</td>
</tr>
<tr>
<td>300x300</td>
<td>126</td>
</tr>
<tr>
<td>400x400</td>
<td>71</td>
</tr>
<tr>
<td>500x500</td>
<td>45</td>
</tr>
</tbody>
</table>
Miscut

Perfect cut leads to an unstable surface
Roughening results
Commercial Wafers are miscut to avoid roughening
Orientation, Conductivity and Resistivity Check

Hot Point Probe
Indicates Majority Charge Carriers
Orientation, Conductivity and Resistivity Check

4 Point Probe allows simultaneous measurement of current and voltage along a distance on a wafer.

Allows to deduce dopant concentration.
Rod Grinding

Figure 3.16  Crystal flat grinding.

Figure 3.17  Wafer flat locations.
**Ingot Characterization**

Single crystal silicon ingots are characterized by the orientation of their silicon crystals. Before the ingot is cut into wafers, one or two "flats" are ground into the diameter of the ingot to mark this orientation.

**Wafer Slicing**

After characterization, wafer producers (Komatsu Silicon America, MEMC, Mitsubishi Silicon America) slice the ingot into individual wafers with a precision "ID Saw," so named because the cutting edge of the blade is on the inside. This type of saw is used because the blade produces more precise and controllable cut and a flatter wafer.
**Edge Profiling**

The larger the wafer, the more center dies are not affected by dislocations.
**Wafer Lapping**
The sliced wafers are mechanically lapped using a counter-rotating lapping machine and an aluminum oxide slurry. This flattens the wafer surfaces, makes them parallel and reduces mechanical defects like saw markings.
**Etching**

**Wafer Etching**

After lapping, wafers are etched in a solution of nitric acid, acetic acid or sodium hydroxide to remove microscopic cracks or surface damage created by the lapping process. The acid or caustic solution is removed by a series of high-purity RO/DI water baths.
**Wafer Polishing**

Next, the wafers are polished in a series of a combination chemical and mechanical polishing processes. **CMP Polishing**

The wafers are held in a hard ceramic chuck using either wax bonding or vacuum and buffed with a slurry of silica powder, RO/DI water and sodium hydroxide.

The polishing process usually involves two or three polishing steps with progressively finer slurry and intermediate cleanings using RO/DI water.
Orientation, Conductivity and Resistivity Check

X-rays are reflected from one end of the polished rod and the reflection pattern reveals the orientation.

Most wafers are aligned at a few degrees off the [100] orientation, some are close to [111].

This is important for ion implantation.
# Industrial Specs

## TABLE 2.3 Specifications for Polished Monocrystalline Silicon Wafers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>125 mm</th>
<th>150 mm</th>
<th>200 mm</th>
<th>300 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter (mm)</td>
<td>125 ± 1</td>
<td>150 ± 1</td>
<td>200 ± 1</td>
<td>300 ± 1</td>
</tr>
<tr>
<td>Thickness (mm)</td>
<td>0.6–0.65</td>
<td>0.65–0.7</td>
<td>0.715–0.735</td>
<td>0.755–0.775</td>
</tr>
<tr>
<td>Primary flat length (mm)</td>
<td>40–45</td>
<td>55–60</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Secondary flat length (mm)</td>
<td>25–30</td>
<td>35–40</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Bow (µm)</td>
<td>70</td>
<td>60</td>
<td>30</td>
<td>&lt; 30</td>
</tr>
<tr>
<td>Total thickness variation (µm)</td>
<td>65</td>
<td>50</td>
<td>10</td>
<td>&lt; 10</td>
</tr>
<tr>
<td>Surface orientation</td>
<td>(100) ± 1°</td>
<td>Same</td>
<td>Same</td>
<td>Same</td>
</tr>
<tr>
<td></td>
<td>(111) ± 1°</td>
<td>Same</td>
<td>Same</td>
<td>Same</td>
</tr>
</tbody>
</table>

NA, not available.
Backsurface Treatment

Trapping/Gettering: sandblasting of the back surface to getter and pin defects and impurities (small wafers)

Polish/Planarization: allowing precise alignment of the front surface by means of attachment to the back surface (large wafers)
Denuding

Remember the segregation coefficients!
If we heat a wafer in N₂ to melt at the surface, oxygen will accumulate in the solid phase.
After cooling, the surface layer is oxygen depleted (purer).
Figure 2.19  Denuded zone width for two sets of processing conditions. Inset shows a schematic of the denuded zone and gettering sites in a wafer cross section.
**Wafer Epitaxial Processing.**

Substrate suppliers use a process called epitaxy (EPI) to grow a layer of single crystal silicon from vapor onto a single crystal silicon substrate at high temperatures. Trichlorosilane or silicon tetrachloride and hydrogen are combined with either diborane or phosphine gas to act as dopants.
The purpose of EPI growth is to create a layer with different, usually lower, concentration of electrically active dopant on the substrate. For example, an n-type layer on a p-type wafer.

Required for CMOS
Short illustration movies
**Silicon**

**Silicon: basic information and properties.**

- Atomic Weight: 28.09
- Electron configuration: [Ne] 3s^2 3p^2
- Crystal structure: Diamond
- Lattice constant (Ångstrom): 5.43095
- Density, atoms/cm^3: 4.995E+22
- Density (g/cm^3): 2.328
- Dielectric Constant: 11.9
- Density of states in conduction band, N_C (cm^-3): 3.22E+19
- Density of states in valence band, N_V (cm^-3): 1.83E19
- Effective Mass, m*/m_0:
  - Electrons: 0.98
  - Holes: 0.19
  - Effective mass m_i^*:
    - Electrons: 0.16
    - Holes: 0.49
- Electron affinity, x(V): 4.05
- Energy gap (eV) at 300K: 1.12
<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic carrier conc. (cm(^{-3}))</td>
<td>1.0E10</td>
</tr>
<tr>
<td>Intrinsic Debye Length (micron)</td>
<td>24</td>
</tr>
<tr>
<td>Intrinsic resistivity (ohm cm)</td>
<td>2.3 E+05</td>
</tr>
<tr>
<td>Linear coefficient of thermal expansion (1(^\circ)C)</td>
<td>2.6 E-06</td>
</tr>
<tr>
<td>Melting point (C)</td>
<td>1415</td>
</tr>
<tr>
<td>Minority carrier lifetime (s)</td>
<td>2.5 E-03</td>
</tr>
<tr>
<td>Mobility (cm(^2)/V sec)</td>
<td></td>
</tr>
<tr>
<td>(\mu) (electrons)</td>
<td>1500</td>
</tr>
<tr>
<td>(\mu) (holes)</td>
<td>450</td>
</tr>
<tr>
<td>Optical-phonon energy (eV)</td>
<td>0.063</td>
</tr>
<tr>
<td>Phonon mean free path (Angstrom)</td>
<td></td>
</tr>
<tr>
<td>Specific heat (J/g (^\circ)C)</td>
<td>0.7</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm (^\circ)C)</td>
<td>1.5</td>
</tr>
<tr>
<td>Thermal diffusivity (cm(^2)/s)</td>
<td>0.9</td>
</tr>
<tr>
<td>Vapor pressure (Pa)</td>
<td>1 at 1650C</td>
</tr>
<tr>
<td></td>
<td>1E-6 at 900 C</td>
</tr>
<tr>
<td>Index of refraction</td>
<td>3.42</td>
</tr>
<tr>
<td>Breakdown field (V/cm)</td>
<td>~3 E+05</td>
</tr>
</tbody>
</table>
### Silicon: Important property summary & comparison

Comparison of properties of selected SiC polytypes with silicon and GaAs (\(T = 300\,\text{K}\)).

<table>
<thead>
<tr>
<th>Property</th>
<th>Silicon</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
<th>3C-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.1</td>
<td>1.42</td>
<td>3.2</td>
<td>3.0</td>
<td>2.3</td>
</tr>
<tr>
<td>Relative dielectric constant</td>
<td>11.9</td>
<td>13.1</td>
<td>9.7</td>
<td>9.7</td>
<td>9.7</td>
</tr>
<tr>
<td>Breakdown field at (N_d = 10^{13},\text{cm}^{-3}) (MVcm(^{-1}))</td>
<td>0.6</td>
<td>0.6</td>
<td>(\parallel\text{c-axis: 3.0})</td>
<td>(\parallel\text{c-axis: 3.2,})</td>
<td>(\perp\text{c-axis: &gt; 1})</td>
</tr>
<tr>
<td>Thermal conductivity (W cm(^{-1})K(^{-1}))</td>
<td>1.5</td>
<td>0.5</td>
<td>3–5</td>
<td>3–5</td>
<td>3–5</td>
</tr>
<tr>
<td>Intrinsic carrier concentration (cm(^{-3}))</td>
<td>(10^{19})</td>
<td>(1.8 \times 10^6)</td>
<td>(\sim 10^{-7})</td>
<td>(\sim 10^{-5})</td>
<td>(\sim 10)</td>
</tr>
<tr>
<td>Electron mobility at (N_d = 10^{16},\text{cm}^{-3}) (cm(^2)V(^{-1})s(^{-1}))</td>
<td>1200</td>
<td>6500</td>
<td>(\parallel\text{c-axis: 800,})</td>
<td>(\parallel\text{c-axis: 60,})</td>
<td>750</td>
</tr>
<tr>
<td>Hole mobility at (N_A = 10^{16},\text{cm}^{-3}) (cm(^2)V(^{-1})s(^{-1}))</td>
<td>420</td>
<td>320</td>
<td>115</td>
<td>(\perp\text{c-axis: 800})</td>
<td>(\perp\text{c-axis: 400})</td>
</tr>
<tr>
<td>Saturated electron velocity (10(^{5}) cm s(^{-1}))</td>
<td>1.0</td>
<td>1.2</td>
<td>2</td>
<td>2</td>
<td>2.5</td>
</tr>
<tr>
<td>Donor dopants and shallowest ionization energy (meV)</td>
<td>P: 45, As: 54</td>
<td>Si: 5.8</td>
<td>N: 45, P: 80</td>
<td>N: 85, P: 80</td>
<td>N: 50</td>
</tr>
<tr>
<td>Acceptor dopants and shallowest ionization energy (meV)</td>
<td>B: 45</td>
<td>Be, Mg, C: 28</td>
<td>Al: 200, B: 300</td>
<td>Al: 200, B: 300</td>
<td>Al: 270</td>
</tr>
<tr>
<td>Commercial wafer diameter as of 1999 (cm)</td>
<td>30</td>
<td>15</td>
<td>5</td>
<td>5</td>
<td>None</td>
</tr>
</tbody>
</table>

**Sources:** Sze (1981), Harris (1995), Choyke et al. (1997), Pend et al. (1998)
Crystal structure of silicon (diamond structure).
**Consistency check:**

Unit cell: 8 atoms at corners at 1/8 each in cell
6 atoms in faces at ½ each in cell
4 atoms within cell.
Thus total of 8 Si atoms per unit cell.

Each Si atom weighs 28 atomic mass units (1.66 E-24 grams). Dimension of unit cell is 5.43 angstroms or 5.43 E-08 cm.

Thus density should be:

\[
\frac{8 \text{atoms} \times 28 \text{amu} / \text{atom} \times (1.66e - 24) \text{g} / \text{amu}}{(5.43e - 08 \text{cm})^3} = 2.32 \text{g} / \text{cm}^3
\]

Agrees with measured density of 2.33 g/cm³
Crystal planes of Silicon and Miller Indexes.

Start with unit cell.
Plane can be defined in terms of intercepts along 3 unit cell axes.

\[
\frac{x}{\alpha} + \frac{y}{\beta} + \frac{z}{\gamma} = 1
\]
Miller Indexes.

Miller indexes that define plane are inverse of $\alpha, \beta, \gamma : h, k, l$. The plane is then designated (hkl). The set of symmetrically equivalent planes is designated \{hkl\}. The direction normal to the plane is often designated [hkl]. The set of equivalent directions is $<hkl>$. Planes can involve multiple cells:

- Negative direction denoted by line above miller index.
- Fractions are usually rationalized.

![Miller Indexes Diagram]
Miller indexes for silicon: examples.

(111) Plane

(110) Plane

Set of (120) planes
**Crystal defects in Silicon: Point defects**

i). Large substitutional impurity.
f). Small substitutional impurity.
c). Interstitial silicon atom.
a). Interstitial impurity.
g). Vacancy
Crystal Defects: Line defects
Example: edge dislocation

Crystal Defects: Area defects
Grain boundaries.
Surfaces.
....more...

Crystal Defects: Volume defects
Precipitates.
Voids.
....more...
Why bother about defects?

Change electronic properties
  Recombination, Band Bending
Change chemical properties
  Etch rate, Long-Time Resistance
Change mechanical properties
  Thermal expansion