Text Book:
Silicon VLSI Technology
Fundamentals, Practice and Modeling
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CMOS TECHNOLOGY

- We will describe a modern CMOS process flow.

- Typical CMOS technologies in manufacturing today add additional steps to implement multiple device $V_{TH}$, TFT devices for loads in SRAMs, capacitors for DRAMs etc.

- Process described here requires 16 masks and > 100 process steps.

- There are many possible variations on the process flow described here, some of which are described in Chapter 2 in the text. e.g. see the STI section in the text.
CMOS Digital Gates

- In the simplest CMOS technologies, we need to realize simply NMOS and PMOS transistors for circuits like those illustrated below.
P-well Fabrication

- Photolithography
  - Mask #2 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Ion Implantation
  - B+ ion bombardment
  - Penetrate thin SiO₂ and field SiO₂
  - 150-200 KeV for $10^{13}$ cm⁻²
    - Implantation Energy and total dose adjusted for depth and concentration

- Strip Photoresist
N-well Fabrication

- Photolithography
  - Mask #3 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Ion Implantation
  - P+ ion bombardment
  - Penetrate thin SiO₂ and field SiO₂
  - 300-400 KeV for 10¹³ cm⁻²
    - Implantation Energy and total dose adjusted for depth and concentration

- Strip Photoresist
Thermal Anneal and Diffusion

- Thermal Anneal
  - Repair crystal lattice structure damage due to implantation
- N and P Drive-in
  - Thermal diffusion of dopant to shallower than desired depth
    - Drive-in is a cumulative process!
- Dry Furnace (N₂ ambient)
  - Anneal
    - 30 min @ 800°C or
    - RTA 10 sec @ 1000°C
  - Drive-in
    - 4-6 hours @ 1000 °C - 1100 °C
Threshold Adjustment, P-type NMOS

\[ V_{TH} = V_{FB} + 2\Phi_f + \frac{\sqrt{2e\Phi_f N_i(2\Phi_f)}}{C_{OX}} + \frac{qQ_d}{C_{OX}} \]

- Photolithography
  - Mask #4 pattern alignment and UV exposure
  - Rinse away non-pattern PR
- Ion Implantation
  - B+ ion bombardment
  - 50-75KeV for 1-5 \times 10^{12} \text{ cm}^{-2}
    - Implantation Energy and total dose adjusted for depth and concentration
- Strip Photoresist
Threshold Adjustment, N-type PMOS

- Photolithography
  - Mask #5 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Ion Implantation
  - As⁺ ion bombardment
  - 75-100 KeV for 1-5 x 10¹² cm⁻²
    - Implantation Energy and total dose adjusted for depth and concentration

- Strip Photoresist
Gate Oxide Growth

- Remove existing gate region oxide
  - HF etch

- Furnace Steps
  - Thermal Anneal
    - Dry Furnace (N₂ ambient)
    - 30 min @ 800°C
  - Oxide growth 3-5 nm
    - O₂ ambient
    - 0.5-1 hour @ 800°C
Polysilicon Gate Deposition

- LPCVD Deposition of Si
  - Silane
    \[ \text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2 \]
- Amorphous or polycrystalline silicon layer results
  - 0.3-0.5 um
- Ion Implantation
  - P+ or As+ (N+) implant dopes the poly
    (typically \(5 \times 10^{15} \text{ cm}^{-2}\))
Gate Patterning

- Photolithography
  - Mask #6 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Plasma Etch
  - Anisotropic etch
    - Vertical etch rate high
    - Lateral etch rate low
  - Chlorine or Bromine based for SiO₂ selectivity
Extension (LDD) Formation NMOS

- Photolithography
- Mask #7 pattern alignment and UV exposure
- Rinse away non-pattern PR

- Ion Implantation
  - P+ ion bombardment
  - 50 KeV for $5 \times 10^{13} \text{ cm}^{-2}$

- Strip Photoresist

LDD:
- Lightly Doped Drain
- Reduce short channel effects due to gate voltage magnitudes and electric fields
- Source and Drain must be layered as NMOS:N+N-P or PMOS: P+P-N
Extension (LDD) Formation PMOS

- Photolithography
- Mask #8 pattern alignment and UV exposure
- Rinse away non-pattern PR

- Ion Implantation
  - B+ ion bombardment
  - 50 KeV for $5 \times 10^{13} \text{ cm}^{-2}$

- Strip Photoresist
SiO$_2$ Spacer Deposition

- CVD or LPCVD Deposition of SiO$_2$
- Silane and Oxygen
  \[ \text{SiH}_4 + \text{O}_2 \rightarrow \text{SiO}_2 + 2\text{H}_2 \]
- Or
  \[ \text{SiH}_2\text{Cl}_2 + \text{N}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{N}_2 + 2\text{HCl} \]
- 0.5 um
- Provides spacing between gate and source-drain.
- Reduce field at gate edge
Anisotropic Spacer Etch

- Photolithography
  - Mask #6 oversized pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Plasma Etch
  - Anisotropic etch
    - Vertical etch rate high
    - Lateral etch rate low
  - Flourine based

- Strip Photoresist
NMOS Source and Drain Implant

- Screen Oxide Growth
  - Thin SiO2 layer ~10 nm to scatter the implanted ions
  - Reduce channeling

- Photolithography
  - Mask #9 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Ion Implantation
  - As+ ion bombardment
  - 75 KeV for 2-4 x 10^{15} cm^{-2}

- Strip Photoresist
PMOS Source and Drain Implant

- Photolithography
- Mask #10 pattern alignment and UV exposure
- Rinse away non-pattern PR

- Ion Implantation
- B+ ion bombardment
- 5-10 KeV for 1-3 x 10^{15}cm^{-2}

- Strip Photoresist
Thermal Annealing

- Thermal Anneal
  - Repair crystal lattice structure damage due to implantation

- N+ and P+ Drive-in
  - Thermal diffusion of dopant to shallower than desired depth
    - Drive-in is a cumulative process!

- Dry Furnace (N₂ ambient)
  - Anneal
    - 30 min @ 900°C or
    - RTA 60 sec @ 1000 °C - 1050 °C

Transient Enhanced Diffusion (TED)
  - Higher than normal diffusivity due to crystal damage
Contact Openings

- HF etch to remove thin SiO₂
- Remove screen oxide from drain, source and ploy gate regions
- Dip for a few seconds

LDD and Sidewall structure
- NMOS: Lateral N+ N- P N- N+
- PMOS: Lateral P+ P- N P- P+
Contacts and Interconnects

- Titanium sputtering local contacts
- Conformal Coat with SiO₂
- Planarization
- Tungsten Plug vias
- Aluminum Metal Deposition
- Repeat
  - Coat
  - Planarize
  - Plug
  - Metal deposition
Titanium Deposition

- Ti is deposited by sputtering (typically 100 nm).
  - Ti target hit with Ar+ ions in a vacuum chamber

- The Ti is reacted in an N\textsubscript{2} ambient,
- Forms TiSi\textsubscript{2} and TiN (typically 1 min @ 600 - 700 °C).
- TiSi\textsubscript{2} has excellent contact characteristics
- TiN does not, but can be used for local wiring
Local TiN Interconnect

- Photolithography
  - Mask #11 pattern alignment and UV exposure
  - Rinse away non-pattern PR
- TiN etch
  - NH4OH:H2O2:H2O (1:1:5)
- Strip Photoresist
- Thermal Treat in Ar
  - 1 min @ 800 °C
Conformal Coat and Planarize

- Conformal layer of SiO₂ is deposited by CVD or LPCVD (typically 1 μm)
  - PSG or BPSG
  - Surface passivation
  - Glass reflow for partial planarization

- Chemical Mechanical Polishing (CMP)
  - Planarize the wafer surface
  - Polish with high pH silica slurry
Vias to 1st Metal

- Photolithography
- Mask #12 pattern alignment and UV exposure
- Rinse away non-pattern PR
- SiO$_2$ plasma etch
- Anisotropic etch
- Strip Photoresist

PMOS

NMOS

N Well

P Well
Via Deposition – Tungsten Plugs

- TiN or Ti/TiN barrier layer
  - Sputtering or CVD (few tens of nm)

- CVD Tungsten (W)
  \[ \text{WF}_6 + 3\text{H}_2 \rightarrow \text{W} + 6\text{HF} \]

- Chemical Mechanical Polishing (CMP)
  - Planarize the wafer surface
  - Polish with high pH silica slurry
Damascene Process

- Etch Contact Holes or Line Trenches
- Fill etched regions
- Planarize
  - CMP process
  - Also removes material that “overflowed holes or trenches

- Also used in reference to copper line metal layer deposition
Metal #1 Deposition

- Photolithography
  - Mask #13 pattern alignment and UV exposure
  - Rinse away non-pattern PR
- Sputtered Aluminum
  - Al with small amounts of Si and Cu
  - Cu reduces electromigration
- Anisotropic plasma etch
- Strip Photoresist
Multiple Metal Layers

- Deposits Oxide Layer
- CMP
- Photolithography Mask #14
- Etch Vias
- Deposit via material
- CMP
- Photolithography Mask #15
- Deposit Next Metal Layer

- Final passivation layer of Si₃N₄ is deposited by PECVD and patterned with Mask #16.

- Final anneal and alloy in forming gas (10% H₂ in N₂)
  - 30 min @ 400-450 °C
2-Level Metal CMOS

PMOS and NMOS wafer cross section after fabrication

CMOS Technology - Chapter 2
• Photos of state-of-the-art CMOS chips (from Intel website).
• 90 nm technology.
**Summary of Key ideas**

- This chapter serves as an introduction to CMOS technology.

- It provides a perspective on how individual technologies like oxidation and ion implantation are actually used.

- There are many variations on CMOS process flows used in industry.

- The process described here is intended to be representative, although it is simplified compared to many current process flows.

- Some process options are described in Chapter 2 in the text.

- Perhaps the most important point is that while individual process steps like oxidation and ion implantation are usually studied as isolated technologies, their actual use is complicated by the fact that IC manufacturing consists of many sequential steps, each of which must integrate together to make the whole process flow work in manufacturing.