Text Book:
Silicon VLSI Technology
Fundamentals, Practice and Modeling
Authors: J. D. Plummer, M. D. Deal, and P. B. Griffin
• Invention of the bipolar transistor - 1947, Bell Labs.

• Shockley’s “creative failure” methodology

• Grown junction transistor technology of the 1950s
History

• Bardeen, Brattain and Shockley
  – Point Contact Transistor in 1947 at Bell Laboratory
  – Followed by the bipolar transistor

• Integrated Circuit Development
  – Jack Kilby demonstrated in 1958
    • Texas Instruments
  – Robert Noyce similar time frame with Silicon
    • Fairchild Semiconductor
Physical Devices

• NPN and PNP Bipolar Junction Transistors
• Field Effect Transistors (FET)
  – Metal-Oxide-Semiconductor FET (MOSFET)
  – Junction FET (JFET)
• Others:
  – PN Junction
  – Resistor
  – Capacitor
  – Photo-Diode and Photo-Transistor
• Alloy junction technology of the 1950s.

• Double diffused transistor technology of the 1950s.
• The planar process (Hoerni - Fairchild, late 1950s).
• First “passivated” junctions.
Photolithography

- Basic lithography process
  - Apply photoresist
  - Patterned exposure
  - Remove photoresist regions
  - Etch wafer
  - Strip remaining photoresist
Planar Integrated Circuit

- Patterning of multiple photoresist patterns and processing steps create a planar integrated circuit
  - P regions
  - N regions
  - Metal Contact Holes
  - Metal Pattern

Analog BJT
Planar Digital IC

- Complimentary Metal-Oxide-Semiconductor (CMOS)
  - N-channel MOS Field Effect Transistors NMOS
  - P-channel MOS Field Effect Transistors PMOS

Mask Layers:
P-well
N-well
P+
N+
Gate
Contact
L1
L1-L2 via
L2
L2-L3 via
L3

PMOS
NMOS
Thickness
Substrate: >500 um
Active Layer: < 1 um

P17
Multiple Metal Layers

- Metal Planarization required for multiple metal layers
  - Metal Deposition
  - Patterning
  - Fill Dielectric
  - Planarization
  - Contact vias
  - Contact Deposition

Figure 1-12 Actual cross section of a modern IC (IBM's PowerPC chip). Note the multiple layers of metal for wiring above the silicon surface. The active parts of the transistors are barely visible at the bottom of the photograph. Reprinted with permission of Integrated Circuit Engineering Corporation.
NEXT TIME:
BASIC DEVICE PHYSICS
Challenges For The Future

• Having a “roadmap” suggests that the future is well defined and there are few challenges to making it happen.

• The truth is that there are enormous technical hurdles to actually achieving the forecasts of the roadmap. Scaling is no longer enough.

• 3 stages for future development:

  “Technology Performance Boosters”

  Invention

  • Spin-based devices
  • Molecular devices
  • Rapid single flux quantum
  • Quantum cellular automata
  • Resonant tunneling devices
  • Single electron devices

Materials/process innovations
NOW

Device innovations
IN 5-15 YEARS

Beyond Si CMOS
IN 15 YEARS??
Broader Impact of Silicon Technology

- Many other applications e.g. MEMs and many new device structures e.g. carbon nanotube devices, all use basic silicon technology for fabrication.
Summary of Key Ideas

• ICs are widely regarded as one of the key components of the information age.

• Basic inventions between 1945 and 1970 laid the foundation for today's silicon industry.

• For more than 40 years, "Moore's Law" (a doubling of chip complexity every 2-3 years) has held true.

• CMOS has become the dominant circuit technology because of its low DC power consumption, high performance and flexible design options. Future projections suggest these trends will continue at least 15 more years.

• Silicon technology has become a basic “toolset” for many areas of science and engineering.

• Computer simulation tools have been widely used for device, circuit and system design for many years. CAD tools are now being used for technology design.

• Chapter 1 also contains some review information on semiconductor materials semiconductor devices. These topics will be useful in later chapters of the text.
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CMOS TECHNOLOGY

- We will describe a modern CMOS process flow.

- Typical CMOS technologies in manufacturing today add additional steps to implement multiple device $V_{TH}$, TFT devices for loads in SRAMs, capacitors for DRAMs etc.

- Process described here requires 16 masks and > 100 process steps.

- There are many possible variations on the process flow described here, some of which are described in Chapter 2 in the text. e.g. see the STI section in the text.
CMOS Digital Gates

- In the simplest CMOS technologies, we need to realize simply NMOS and PMOS transistors for circuits like those illustrated below.
2-Level Metal CMOS

PMOS and NMOS wafer cross section after fabrication
Processing Phases

- Choosing a Substrate
- Active Region
- N and P Well
- Gate
- Tip or Extension
- Source and Drain
- Contact and Local Interconnect
- Multilevel Metalization
Choosing a Substrate

- Substrate selection:
  - moderately high resistivity (25-50 ohm-cm)
  - (100) orientation
  - P- type.

- Initial processing:
  - Wafer cleaning
  - thermal oxidation, $\text{H}_2\text{O}$
    ($\approx 40 \text{ nm}, 15 \text{ min.} \@ 900^\circ\text{C}$)
  - nitride LPCVD deposition
    ($\approx 80 \text{ nm}$)

\[3\text{SiH}_4 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12\text{H}_2\]

1st Mask Photoresist
- spinning and baking
  ($\approx 0.5 - 1.0 \mu\text{m}$)
Active Area Definition

- Photolithography
  - Mask #1 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Dry etch the Nitride layer
  - Plasma etch with Fluorine
    - $CF_4$ or $NF_4$ Plasma
    - $Si_3N_4 + 12F \rightarrow 3SiF_4 + 2N_2$

- Strip Photoresist
Field Oxide Growth

- Wet Oxide (thick SiO$_2$)
  - H$_2$O ($\approx$ 500 nm, 45 min. @ 1000°C)
- LOCOS: Local Oxidation of Silicon
- Strip Nitride layer
  - Phosphoric acid or plasma etch

Instead of Si$_3$N$_4$ use
SiO$_2$/PolySi/Si$_3$N$_4$=
Poly Buffered LOCOS
Results in less bird’s beak
P-well Fabrication

- Photolithography
  - Mask #2 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Ion Implantation
  - B+ ion bombardment
  - Penetrate thin SiO₂ and field SiO₂
  - 150-200 KeV for $10^{13}$ cm$^{-2}$
    - Implantation Energy and total dose adjusted for depth and concentration

- Strip Photoresist
N-well Fabrication

- Photolithography
  - Mask #3 pattern alignment and UV exposure
  - Rinse away non-pattern PR

- Ion Implantation
  - P+ ion bombardment
  - Penetrate thin SiO₂ and field SiO₂
  - 300-400 KeV for 10¹³ cm⁻²
    - Implantation Energy and total dose adjusted for depth and concentration

- Strip Photoresist