Schematic creation of MOS field effect transistor.
Step 0

The positively doped silicon wafer is first coated with an insulating layer of silicon dioxide (yellow) through chemical vapor deposition or thermal oxidation.
Step 1

An ultraviolet light-sensitive thin layer of photoresist (blue) is applied to the silicon dioxide surface and evenly spread across the wafer.
Step 2

The first mask is placed over the wafer and ultraviolet light is projected onto the mask. Areas of photoresist exposed to the light are hardened and those shielded remain soft.

(Lithography step number 1)
Step 3

The unexposed (and soft) photoresist is removed by washing with a solvent, leaving the hardened resist and underlying silicon dioxide layer intact.
Step 4

The upper layer of the silicon dioxide is removed by etching with hot gasses, leaving only a very thin layer for insulation.
Step 5

The hardened photoresist is removed with a chemical solvent leaving an uneven silicon dioxide surface over the entire wafer.
Step 6

A layer of conducting polysilicon is then deposited onto the silicon dioxide surface using chemical vapor deposition. This material will serve as the transistor's gate.
Step 7

A second layer of photoresist is applied over the polysilicon to prepare the wafer's surface for a second photomask.
Step 8

The second mask is placed over the wafer and ultraviolet light is again projected onto the mask. The areas exposed to the light are hardened.

(Lithography step number 2)
Step 9

The unexposed photoresist is washed away with a solvent, leaving only the T-shaped hardened resist on the wafer.
Step 10

The next step is ion-beam milling (etching) to remove the excess polysilicon and another thin layer of silicon dioxide exposing the silicon wafer's surface.
Step 11

The photoresist is removed with solvent leaving a ridge of polysilicon (the transistor's gate), which rises above the silicon wells.
Step 12

Chemical doping implants phosphorous (green) deep within the silicon wells surrounded by the silicon dioxide and polysilicon layers to produce positively doped silicon.
Step 13

A second layer of silicon dioxide is applied to provide insulation of the basic transistor structure from metal contacts to be applied later.
Step 14

A third film of photoresist is added to prepare the formation of vertical shafts (vias) that will contain metal contacts for the polysilicon and the wells.
Step 15

The third mask is illuminated with ultraviolet light, hardening the photoresist everywhere with the exception of small black rectangles that will become shafts.

(Lithography step number 3)
Step 16

Removal of the soft photoresist with solvent exposes three areas of exposed silicon dioxide that mark the planned shafts.
Step 17

The wafer is next etched again to remove silicon dioxide and exposing the positively doped silicon and the polysilicon gate.
Step 18

The remaining photoresist is then washed away with solvent. The positively doped silicon areas (green) will serve as the source and the drain.
Step 19

The wafer is then sputter-coated with aluminum that fills the shafts and evenly coats the wafer's surface to provide electrical contacts.
Step 20

A fourth layer of photoresist is applied to the wafer to prepare the transistor for its final mask, which will produce the pattern for the aluminum "wiring".
Step 21

Ultraviolet light shining through the metallization mask hardens the photoresist covering the aluminum, which will carry current to and from the transistor.

(Lithography step number 4)
Step 22

The unexposed photoresist is removed with solvent, exposing many bare regions of aluminum that will be removed next.
Step 23

A final etching step removes exposed aluminum leaving only the metal necessary to make contacts in the shafts and connectors on the surface.
Step 24

The last resist is washed away with solvent and the transistor is finished, along with millions of its neighbors on the wafer.