Linear Regulators: Fundamentals and Compensation

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February 15, 2012
1 Introduction

2 Review of Linear Regulator Topologies

3 Transfer Functions

4 Poles & Zeros

5 Bode Magnitude & Phase Plots
1. Introduction

2. Review of Linear Regulator Topologies

3. Transfer Functions

4. Poles & Zeros

5. Bode Magnitude & Phase Plots
Introduction to Seminar Series

Goals of the Seminar Series

- Provide an overview of power conversion techniques
  *Power supplies are common subsystems in most of our products*

- Present follow-up seminars in related areas
  → switching regulator topologies/compensation, simulation

- Offer refresher seminars in fundamental areas
  → mathematical modeling, circuit analysis, control design
Previous Seminars

Overview of Linear and Switching Power Supplies

- Two seminars were held on September 15 and October 17, 2005, a total of 83 people attended these seminars.
- Follow-up seminars in linear and switching regulators were requested.

http://compass.mot.com/go/powerconversion
Outline

1. Introduction

2. Review of Linear Regulator Topologies

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5. Bode Magnitude & Phase Plots
Three-terminal devices – input, output, common (ground)

Linear regulators may be classified by their series (pass) transistor
- Series element may consist of bipolar or field-effect transistors

Bipolar outputs → Darlington NPN, PNP, NPN-PNP

Majority of regulators use bipolars (FET-based regulators $)

Series transistor structure determines $V_{\text{dropout}}$, $I_{\text{bias}}$, $I_q$, $P_{\text{diss}}$

Frequency compensation and protection circuitry also important

$V_{\text{dropout}}$ minimum input-output voltage difference to stay in regulation

$I_{\text{bias}}$ bias current for the pass transistor

$I_q$ regulator quiescent current of which $I_{\text{bias}}$ is one component

$P_{\text{diss}}$ regulator power dissipation
Linear Regulator – Typical Usage

- TPS76433 – 3.3V, 150mA, PMOS LDO linear regulator
- Low output voltage noise ($50\mu V$), Low power ($I_q = 140\mu A$)
- $0.01\mu F$ bypass capacitor filters reference voltage
- Capacitor ESR important for stability (not too high, not too low)
- Current limit (1A), thermal protection (165°C shutdown)
NPN Regulator

Characteristics
- NPN Darlington pass
- PNP driver
- Used in 78xx series
- \( I_{bias} \approx \frac{I_{load}}{\beta^3} \)
- Smallest chip area
- Small comp. capacitor
- Least expensive
- \( V_{do} = 2V_{BE} + V_{sat} \approx 2.0V \)
- No reverse battery protection
PNP Low Dropout (LDO) Regulator

Characteristics

- PNP pass
- NPN or EA direct drive
- \( V_{do} = V_{sat} \approx 600\text{mV} \)
- Inherent reverse battery protection
- \( I_{bias} \approx I_{load}/\beta_{pnp} \)
- Large chip area
- Large comp. capacitor
- More expensive
Composite (Quasi-LDO) Regulator

Composite Regulator

Characteristics

- NPN pass
- PNP driver
- $V_{do} = V_{BE} + V_{sat} \approx 1.3V$
- $I_{bias} \approx I_{load}/\beta^2$
- Compromise between NPN and PNP
- Larger chip area than NPN
- Large comp. capacitor
- No reverse battery protection
PMOS LDO Regulator

Characteristics

- PMOS pass
- NPN driver
- Very low $V_{do}$ ($\approx 50\text{mV}$)
- $V_{do}$ controlled by $R_{ds,\text{on}}$
- Very low $I_{bias}$
- Can't enhance FET for $V_{in} < 3V$
NMOS LDO Regulator

Characteristics

- NMOS pass
- Direct drive
- Very low $V_{do}$
- Lower $R_{ds, on}$ than PMOS
- Lower output impedance
- Smaller external caps
- Needs $V_{bias} > V_{out}$ to enhance FET
<table>
<thead>
<tr>
<th>Topology</th>
<th>Advantages</th>
<th>Disadvantages</th>
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<tbody>
<tr>
<td>NPN</td>
<td>smallest die size</td>
<td>large dropout voltage</td>
</tr>
<tr>
<td></td>
<td>fastest transient response</td>
<td>no rev. batt. protection</td>
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<tr>
<td></td>
<td>smallest comp. capacitor</td>
<td></td>
</tr>
<tr>
<td>PNP LDO</td>
<td>low dropout voltage</td>
<td>high quiescent current</td>
</tr>
<tr>
<td></td>
<td>rev. battery protection</td>
<td>large comp. capacitor</td>
</tr>
<tr>
<td></td>
<td>large comp. capacitor</td>
<td>large die size</td>
</tr>
<tr>
<td>NPN/PNP</td>
<td>moderate dropout voltage</td>
<td>large comp. capacitor</td>
</tr>
<tr>
<td></td>
<td>lower $I_q$ than PNP</td>
<td>no rev. battery protection</td>
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<tr>
<td>PMOS LDO</td>
<td>very low $V_{do}$ and $I_{bias}$</td>
<td>need $V_{in} &gt; 3V$</td>
</tr>
<tr>
<td></td>
<td>$V_{do} \propto R_{ds, on}$</td>
<td></td>
</tr>
<tr>
<td>NMOS LDO</td>
<td>very low $V_{do}$, low $R_{out}$</td>
<td>need $V_{bias} &gt; V_{out}$</td>
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<td>lower $R_{ds, on}$ than PMOS</td>
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</table>
Outline

1. Introduction
2. Review of Linear Regulator Topologies
3. Transfer Functions
4. Poles & Zeros
5. Bode Magnitude & Phase Plots
Transfer function is a ratio of response to excitation \( \frac{\text{response}}{\text{excitation}} \).

Use of \( \frac{\text{output}}{\text{input}} \) for TFs is vague (E and R can be at same port).

Expressed in frequency domain using Laplace or Fourier Transforms.

**Voltage Gain (V/V),** \( \omega_c = \frac{1}{RC} \) = corner frequency

\[
A(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = \frac{1}{1 + sRC} = \frac{1}{1 + \frac{s}{\omega_c}}
\]

**Input Impedance (Ω)**

\[
Z_{in}(s) = \frac{v_{in}(s)}{i_{in}(s)} = R + \frac{1}{sC} = R\frac{1 + sRC}{sRC} = R\frac{1 + \frac{s}{\omega_c}}{\omega_c}
\]
Poles & Zeros

- Transfer function is a ratio of two polynomials $A(s) = \frac{\text{num}(s)}{\text{den}(s)}$

- **Poles** are values of $s$ that make $\text{den}(s) = 0$
  - Also called roots or natural frequencies
  - Response to initial conditions, independent of applied excitation
  - Determine stability

- **Zeros** are values of $s$ that make $\text{num}(s) = 0$
  - Also called transmission zeros
  - No impact on stability
  - Determine undershoot, transient response (with poles)

- Evaluate TF by letting $s = j\omega$ and take complex magnitude and phase

\[
A(j\omega) = \frac{1}{1 + j\frac{\omega}{\omega_c}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}} \angle -\tan^{-1}\left(\frac{\omega}{\omega_c}\right)
\]

- **magnitude**
- **phase**
Loop gain $T(s)$ is the product of forward and feedback gains

Closed-loop system can be unstable even if $T(s)$, $G(s)$ have no RHP poles

Undesired ringing and overshoot can occur even in stable systems

Crossover frequency $\omega_c$ is where $\|T(j\omega_c)\| = 1 \Rightarrow 0$ dB

Phase margin $\phi_m = 180^\circ + \angle T(j\omega_c)$

If $\phi_m > 0^\circ \Rightarrow$ feedback system stable (no RHP poles)

Small $\phi_m \Rightarrow$ high-Q resonant poles near $\omega_c \Rightarrow$ overshoot & ringing

We normally need $\phi_m \geq 45^\circ$ in practical feedback systems

If $\phi_m < 0^\circ \Rightarrow$ feedback system unstable (at least one RHP pole)
1st Order Poles and Zeros

1st Order Pole: \( \frac{1}{1+s/\omega_c} \)

- 3dB
- -20dB/dec
- 5.7°
- -45°/dec
- 5.7°

1st Order Zero: 1 + \( s/\omega_c \)

- +20dB/dec
- +45°/dec
- 5.7°
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Bode Plot (magnitude & phase)

Frequency (rad/sec)

Magnitude (dB)

Phase (deg)

-20dB/dec
LDO System (3.3V/100mA)

\[ V_{out} = (1 + \frac{R_1}{R_2}) V_{ref} = (1 + \frac{0.64R}{0.36R}) 1.192V = 3.31V \]

\[ R_L = \frac{V_{out}}{I_{load}} = \frac{3.3V}{100mA} = 33\Omega \]
LDO System Model Simple

\[ G_{pmos} v_{gs} = (g_m r_{ds}) v_{gs} \]

\[ Z_o(s) \approx (R_c + \frac{1}{sC_o}) \parallel \frac{1}{sC_b} \parallel R_L \]

\[ G_{ea} v_s = G_{ea} (v_s - V_{ref}) \rightarrow 0 \]
LDO System Loop Gain

\[ G_{oa}(s) \]

\[ -G_{pmos} \]

\[ G(s) \]

\[ \frac{1}{1+sr_{oa}C_{gs}} \]

\[ -g_m r_{ds} \]

\[ \frac{Z_o(s)}{r_{ds} + Z_o(s)} \]

\[ G_{fb} \]

\[ \frac{R_2}{R_1 + R_2} \]

\[ V_{ref} = 0 \]
LDO System Loop Gain (redrawn)

\[ G_{oa}(s) = \frac{1}{1+sr_{oa}C_{gs}} \]

PMOS Voltage Gain

\[ G_{pmos} \]

Load & Filter

\[ \frac{Z_o(s)}{r_{ds}+Z_o(s)} \]

\[ V_{ref} = 0 \]

Error Amp Gain

\[ G_{ea} \]

Frequency Response

\[ V_{gs} \]

\[ G(s) \]

Feedback Divider

\[ \frac{R_2}{R_1+R_2} \]

\[ G_{fb} \]

\[ T(s) \]

\[ V_{out} \]
Loop Gain Calculation

\[ G(s) \approx G_0 \frac{1 + s/\omega_z}{(1 + s/\omega_o)(1 + s/\omega_b)} \]

with \( G_0 = \frac{R_L}{r_{ds} + R_L} \)

\[ T(s) \approx G_{pmos} G_0 G_{fb} G_{ea} \frac{1 + s/\omega_z}{(1 + s/\omega_o)(1 + s/\omega_b)(1 + s/\omega_{oa})} \]

- \( T_0 = G_{pmos} G_0 G_{fb} G_{ea} \Rightarrow \) Low-frequency loop gain
- \( \omega_o \approx 1/[C_o(R_c + r_{ds}||R_L)] \Rightarrow \) Load pole
- \( \omega_{oa} = 1/[R_{oa}C_{gs}] \Rightarrow \) Pole due to opamp-PMOS interaction
- \( \omega_b \approx 1/[C_b R_c (r_{ds}||R_L)/(R_c + (r_{ds}||R_L))] \Rightarrow \) Pole due to bypass cap
- \( \omega_z = 1/[R_c C_o] \Rightarrow \) Zero due to ESR
### Parameters, Gains, Pole/Zero Locations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{out}$</td>
<td>3.3V</td>
</tr>
<tr>
<td>$R_L$</td>
<td>33Ω</td>
</tr>
<tr>
<td>$R_c$</td>
<td>2Ω</td>
</tr>
<tr>
<td>$g_m$</td>
<td>123mA/V</td>
</tr>
<tr>
<td>$r_{ds}$</td>
<td>65Ω</td>
</tr>
<tr>
<td>$R_1$</td>
<td>64kΩ</td>
</tr>
<tr>
<td>$I_{load}$</td>
<td>100mA</td>
</tr>
<tr>
<td>$R_{oa}$</td>
<td>300kΩ</td>
</tr>
<tr>
<td>$C_o$</td>
<td>10µF</td>
</tr>
<tr>
<td>$C_b$</td>
<td>0.5µF</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>200pF</td>
</tr>
<tr>
<td>$R_2$</td>
<td>36kΩ</td>
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### Transfer Functions

<table>
<thead>
<tr>
<th>$G_{pmos}$</th>
<th>$g_m r_{ds}$</th>
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<tr>
<td>$G_{fb}$</td>
<td>$R_1 / (R_1 + R_2)$</td>
</tr>
<tr>
<td>$G_o$</td>
<td>$R_L / (r_{ds} + R_L)$</td>
</tr>
<tr>
<td>$G_{ea}$</td>
<td>N/A</td>
</tr>
<tr>
<td>$T_0$</td>
<td>$G_{pmos} G_0 G_{fb} G_{ea}$</td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>Frequency</th>
<th>Value</th>
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<tbody>
<tr>
<td>$\omega_o$</td>
<td>$1 / [C_o (R_c + r_{ds}</td>
</tr>
<tr>
<td>$\omega_{oa}$</td>
<td>$1 / [R_{oa} C_{gs}]$</td>
</tr>
<tr>
<td>$\omega_b$</td>
<td>$1 / [C_b R_c</td>
</tr>
<tr>
<td>$\omega_z$</td>
<td>$1 / [R_c C_o]$</td>
</tr>
</tbody>
</table>

- $G_{pmos} \Rightarrow 18.1\text{dB}$
- $G_{fb} \Rightarrow -8.9\text{dB}$
- $G_o \Rightarrow -9.45\text{dB}$
- $G_{ea} \Rightarrow 35\text{dB}$
- $T_0 \Rightarrow 34.7\text{dB}$

- $\omega_o \Rightarrow 667\text{Hz}$
- $\omega_{oa} \Rightarrow 2.65\text{kHz}$
- $\omega_b \Rightarrow 172\text{kHz}$
- $\omega_z \Rightarrow 8\text{kHz}$
Conclusion

- item 1
- item 2
- item 3
- item 4
- item 5
References

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