Vita and Publications

SHANTANU DUTT
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Education

1. Ph.D. in Computer Science and Engineering, University of Michigan, Ann Arbor, August 1990.
2. M.Tech. in Computer Engineering, Indian Institute of Technology, Kharagpur, India, December 1984.
3. B.E. in Electronics and Communication Engineering, M.S. University of Baroda, Baroda, India, July 1983.

Research Interests

1. VLSI CAD: Physical Design, Physical Synthesis, Logic Synthesis, High Level Synthesis
2. Discrete Optimization
3. Computer Security and Trusted IC Design
4. Bioinformatics
5. FPGA Testing
6. Fault-Tolerant and Dependable Computing – Systems and Chips
7. Parallel Computing

Courses Taught

(1) Computer Organization and Design; (2) Introduction to Logic Design; (3) Digital System Design; (4) CAD-Based Logic Design (incorporates and teaches VHDL); (5) Fault-Tolerant Computing; (6) VLSI Design Automation; (7) Parallel Processing and Architectures.

Work Experience

1. Professor, ECE Department, University of Illinois at Chicago, (8/16/09 -)
2. Associate Professor, EECS/ECE Department, University of Illinois at Chicago, (6/97 - 8/15/09)
3. Senior Consultant, Cadence Design Systems (world's largest VLSI CAD company), summer, 1996.
4. Assistant Professor, EE Department University of Minnesota, Minneapolis (9/90 -5/97).
5. Research and Development Engineer, at Research Center, CMC Ltd., Secunderabad, India, (1985).

Awards and Recognitions

1. **Invited Speaker**, IBM Austin Research Labs, Sept. 2009.
2. **Featured Speaker Recognition** (1 of 2) at the 2006 *Int'l Conference on CAD (ICCAD)* for the paper ""A Network-Flow Approach to Timing-Driven Incremental Placement for ASICs", (ICCAD is a premier refereed conference for VLSI CAD and testing with about a 25% acceptance rate)
3. **Research Award**, UIC College of Engineering, 2007.
4. **Best paper award nomination** for the paper:
   "Efficient On-Line Testing of FPGAs with Provable Diagnosabilities", *Design Automation Conference*, 2004, pp. 498-503. The *Design Automation Conference* is a premier conference on VLSI CAD and testing.
5. **Invited article:** S. Dutt, F. Rota, F. Trovo and F. Hanchek, "Fault Tolerance in Computer Systems–From Circuits to Algorithms", invited article, in *Electrical Engineering Handbook*, Academic Press, 2004.
6. **Invited by Intel** to spend summer of 1999 as a senior consultant at the Strategic CAD Lab, Hillboro, OR–declined due to prior commitments.
7. **Textbook appearance** of our paper:
   S. Dutt, New faster Kernighan-Lin-type graph-partitioning algorithms, *Proc. IEEE/ACM International Conference on CAD*, Nov. 1993. pp 370-377 in the textbook:
   Sabih H. Gerez, *Algorithms for VLSI Design Automation*, Wiley, 1998.
8. **Invited article:** S. Dutt and D. Boley, "Roundoff Errors", invited article, in Wiley Encyclopedia of Electrical and Electronics Engineering, Vol. 18, 1999, pp. 617-627.
9. **Invited by Cadence Design Inc.**, the largest CAD company in the world to spend the summer of 1996 as a senior consultant at their main location in Milpitas, California. Accepted the invitation.
10. **Best Paper award** for the paper:
    S. Dutt and W. Deng, "A probability-based approach to VLSI circuit partitioning", *Proc. Design Automation Conference*, June 1996, pp. 100-105. The *Design Automation Conference* is a premier conference on VLSI CAD and testing.
11. **Most influential paper award** for the first 25 years (1971-1995) of the premier conference on fault tolerance, *The Fault Tolerant Comput. Symp.*, for the paper:
    S. Dutt and J.P. Hayes, "Design and reconfiguration strategies for near-optimal k-fault-tolerant tree architectures", *Proc. Eighteenth Fault Tolerant Comput. Symp.*, June 1988, Tokyo, pp. 328-333
12. **Invited paper:** N.R. Mahapatra and S. Dutt, "New anticipatory load balancing strategies for scalable parallel best-first search", *DIMACS workshop on Parallel Processing of Discrete Optimization Problems*, April 1994.
13. **Textbook appearance** of our research in parallel processing and load balancing, in particular our paper:
    S. Dutt and N.R. Mahapatra, "Scalable load-balancing strategies for parallel A algorithms", Special Issue on Scalability of Parallel Algorithms and Architectures, *Journal of Parallel and Distr. Computing*, Sept. 1994, pp. 488-505 in the textbook:
    V. Kumar, A. Grama, A. Gupta and G. Karypis, "Introduction to Parallel Computing: Design and Analysis of Algorithms," *Benjamin/Cummings Publishing Company*, Redwood City, CA, 1994.
14. **Course reference:** Our research in parallel processing and load balancing has also appeared in a the course: Parallel/Distributed Artificial Intelligence Course, The University of Texas at Arlington, TX (http://ranger.uta.edu/~cook/pai/pai.html). Two of our papers are given as online paper references in this course webpage (out of a total of six online paper references).
15. **Research Initiation Award** from NSF for "Efficient Design of Fault-Tolerant Multiprocessors", 9/92 - 2/96.

Invited Addresses and Colloquia

1. "Efficient design of fault-tolerant multicomputers", Cray Research, Chippewa Falls, Wisconsin, July 1992.
2. "New anticipatory load balancing strategies for scalable parallel best-first search", Workshop on Parallel Processing of Discrete Optimization Problems, DIMACS, Rutgers University, New Jersey, April 1994.
3. "A probabilistic approach to VLSI circuit partitioning", Cadence Design Systems, San Jose, CA, June 1995.
4. "Node-covering, error-correcting codes and multiprocessors with very high average fault tolerance", CRHC Seminar, University of Illinois, Urbana-Champaign, Illinois, Sept. 1995.
5. "New anticipatory load balancing strategies for scalable parallel best-first search", EDRC Seminar, Carnegie-Mellon University, Pittsburgh, Sept. 1995.
6. "A probabilistic approach to VLSI circuit partitioning", SRC CAD Center Seminar, Carnegie-Mellon University, Pittsburgh, Sept. 1995.
7. "Node-covering, error-correcting codes and multiprocessors with very high average fault tolerance", ECE Seminar, University of Texas, Austin, Texas, Sept. 1995.
8. "Node-covering, error-correcting codes and multiprocessors with very high average fault tolerance", CS Seminar, Texas A&M University, College Station, Texas, Sept. 1995.
9. "New Algorithms for VLSI Circuit Partitioning and Placement for Area, Timing and Power Optimization", Texas Instruments, Dallas, May 1996.
10. "New Algorithms for VLSI Circuit Partitioning and Placement for Area, Timing and Power Optimization", IBM Rochester, July 1996.
11. "On-Chip Reconfiguration for Defect and Fault Tolerance of FPGAs", Xilinx Corp., San Jose, CA, August 1996.
12. "A New Approach to Timing-Driven Partitioning and Placement with On-the-Fly Buffer Insertion", Cadence Design Systems, Inc., San Jose, CA, Sept. 1996.
13. "Scalable, High-Performance Parallel Computing for Combinatorial Optimization Problems", Northwestern University, Nov. 1997.
14. "A Stochastic Approach to Timing-Driven Partitioning and Placement with Accurate Net and Gain Modeling", Intel Corp., Hillsboro, OR, Feb. 1998.
15. "Tackling Multiple Design Requirements at the Onset of Physical Design : Constraint- and Operator-Based Partitioning and Placement", Intel Physical Design Research Seminar, Integration: From Synthesis to Layout to Interconnect Design and Analysis, Santa Clara, CA, April 1998.
16. "Tackling Multiple Design Requirements at the Onset of Physical CAD: Constraint-Driven Partitioning and Placement", Computer Engineering Seminar, Univ. of Wisconsin-Madison, Oct. 1998.
17. "Efficient Incremental Rerouting for Fault Reconfiguration in Field Programmable Gate Arrays", CAD Seminar, Northwestern Univ., March 2000.
18. "BIST for Hard Faults, Soft Errors and Tampering in FPGA Circuits", IDA/DARPA Workshop on Trusted ICs, Aug. 2005.
19. "Timing Driven Incremental Physical Design and Other Stories", Univ. of California at San Diego, May 2006.
20. "Discretized Network Flow: A New Efficient Discrete Optimization Technique and its Application to EDA and Other Hard Problems", IBM Austin Research Labs, Sept. 2009.

Funding

1. NSF, "Algorithms for Simultaneous Exploration of Multi-Domain Transforms for Design Closure in Emerging Technologies", (S. Dutt, PI), $250,000, 08/08 to 07/11.
2. Raytheon/DARPA, "ECC based Trusted FPGA Design", (S. Dutt, PI), $200,000, **offered** for period 06/08 to 09/08.
   Note: This funding was offered and an official RFQ sent. However, the SOW was too dense for a 4 month period (June '08 - Sept. '08) for which it was offered. Subsequent negotiations for an amended SOW and funding amount was unsuccessful. This is being listed here to note our success in having the above funding offered that was based on months of interaction and proof-of-concept demonstrations to Raytheon. RFQ available on request.
3. NSF, "Incremental Placement and Routing Algorithms for FPGA and VLSI Circuits", (S. Dutt, PI), $298,000 (approx), 01/03 to 12/08.
4. AFOSR for "MURI: The effects of radio-frequency pulses on electronic circuits and systems", (P. Uslenghi PI, S. Dutt is one of several co-PIs), $4M (approx,). S. Dutt's portion $169K (approx.), 5/01 to 4/06.
   NOTE: S. Dutt's research in this project will involve fault analysis of computer systems penetrated by EM radiation, and analysis of program error manifestations (data, control, crashes, etc.) of such faults via algorithm-based fault tolerance and control-flow monitoring techniques.
5. NSF for "Highly Parallel Branch-and-Bound Algorithms for Solving Optimization Problems", NSF-INRIA Collaborative Research, (with Prof. Vipin Kumar, Dept. of Computer Science, as co-PI), $27,000, 01/96 to 12/99, extended to 02/02.
6. Xilinx Corp. for "Defect-Tolerant FPGAs for Yield Enhancement", approx. $89,000, period 8/97 to 8/04.
7. Univ. of Illinois CRB grant for "New Directions in VLSI Circuit Partitioning and Placement for Power and Area Optimization", $13,333, 01/98 to 12/98.
8. Darpa for "On-line FPGA Testing and Reconfiguration for Fault Tolerance", total amount approx. $1.5M, S. Dutt's portion: $ 465,057, 8/98 to 7/01.
9. Intel Corp. for "Novel Partitioning-Based Placement Methodologies for Timing Optimization in Deep Sub-Micron VLSI", $40,000, 8/98 to 12/99.
10. Intel Corp. equipment grant, four workstations with 550 MHz Xeon processors (approx. $14,000).
11. NSF Research Initiation Award for "Efficient Design of Fault-Tolerant Multiprocessors" $ 100,000, 09/92 to 08/95.
12. Five grants from the U. of Minn. Graduate School for a total of about $40,000. These grants are awarded on a competitive basis across the university; the success rate is less than 25%.

Students Advised

Ph.D. Students–Current

1. *Huan Ren*, Ph.D. Thesis Area: VLSI CAD–Physical Synthesis; prelims defense in Oct. 2008. Ph.D. expected 2010.
2. *Yongzhi Qu*, Ph.D. Thesis Area: Trust Design for FPGAs and ASICs. Ph.D. expected 2014.
3. *Ataul Russel* (joining in Fall 2010), Ph.D. Thesis Area: VLSI CAD. Ph.D. expected 2015.

Ph.D. Students–Past

1. *Hasan Arslan*, graduated, Oct. 2004.
   Ph.D. Thesis: "Incremental Routing Algorithms for FPGA and VLSI Circuits".

2. *Nihar R. Mahapatra*, graduated, August 1996.
   Ph.D. Thesis: "Highly Scalable Parallel Branch-&-Bound Algorithms for Solving Large Optimization Problems".
   Employment: Associate Professor, Dept. of Electrical and Computer Engineering, Michigan State Univ., East Lansing.
3. *Fran Hanchek*, graduated May 1997.
   Ph.D. Thesis: "Design of Fault-Tolerant Arithmetic Circuits and FPGAs".
   Employment: Senior Engineer, Intel Corp., Portland, Oregon.

M.S. Thesis Students–Past

1. *Marco Maggioni*, Dec. 2008..
   M.S. Thesis Topic: "FPGA Trust Design".
2. *Michele Santoro*, expected graduation Dec. 2008.
   M.S. Thesis Topic: "Layout-Driven High Level Synthesis".
3. *Roberto Palazzo*, May 2006, M.S. Thesis: "Interconnect-Driven High Level Synthesis using Isomorphic Mappings of 2-level DFGs". Employment: Completing his remaining M.S. studies at Polytecnico di Milano, Italy.
4. *Vishal Suthar*, July 2005, M.S. Thesis: "Effective BIST Methods for Mixed PLB and Interconnect Test and Diagnosis Sans Fault-Free Assumptions". Employment: Xilinx Inc., San Jose, California.
5. *Paolo Pellegrino*, Dec,. 2004.
   M.S. Thesis Topic: An Internal Microarchitecture Watchdog: Control Flow Checking of Instruction Processing". Employment: Doing his Ph.D. at Polytecnico di Torino, Italy.
6. *Franco Trovo*, Dec. 2002, M.S. Thesis: "Concurrent Control Flow Checking with Micro Rollback in a CISC Processor", Dec. 2002.
7. *Frederico Rota*, Dec. 2002, M.S. Thesis: "Control Flow Checking Using Main Memory Bus Monitoring in an Internal Cache Environment", Dec. 2002. Employment: Internship in Japan.
8. *Vinay Verma*, Sept. 2000, M.S. Thesis: "Incremental Rerouting Algorithms for Field Programmable Gate Arrays", Univ. of Illinois, Chicago. Employment: Xilinx Inc., San Jose, California.
9. *Vimal Shanmugavel*, 1998, M.S. Thesis: "Low-Overhead Reconfiguration for Fault Tolerance in FPGAs", Univ. of Illinois, Chicago. Employment: Tellabs, Chicago.
10. *Halim Theny*, 1997. M.S. Thesis: "Further Advances in Partitioning and Placement of VLSI Circuits". Employment: Intel Corp., Santa Clara, CA.
11. *Scott Vanderlinde*, 1996, M.S. Thesis: "Optical Interconnects for Parallel Computers".
12. *Nam Trinh*, 1995. M.S. Thesis: "Performance comparisons between k-ary n-cubes for divide-and-conquer parallel algorithms". Employment: Anderson Consulting, Mnpls, MN.
13. *Timothy Hartley*, 1995, M.S. Thesis: "A test-bed for simulating reconfiguration in structurally fault- tolerant multicomputers." Employment: AT Corp., Mnpls, MN.
14. *Wenyong Deng*, Oct. 1995. M.S. Thesis: "New Algorithms for VLSI Circuit Partitioning for Area and Timing Optimization". Employment: Cadence Design Systems, San Jose, CA.
15. *Mateen Malik Ahmed*, Nov. 1994. M.S. Thesis: "Design and simulation of a new multicomputer routing switch." Employment: Motorola, Pakistan.
16. *Nihar R. Mahapatra*, June 1993. M.S. Thesis: "Scalable work distribution and duplicate pruning strategies for parallel A* algorithms". Employment: See above.

External Professional Activities

1. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2010.
2. item Program Committee member, *IEEE/ACM Int'l Conf. on CAD (ICCAD)*, 2009.
3. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2009.
4. Session Chair, *IEEE/ACM Int'l Conf. on CAD (ICCAD)*, 2008.
5. Program Committee member, *IEEE/ACM Int'l Conf. on CAD (ICCAD)*, 2008.
6. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2008.
7. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2007.
8. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2006.
9. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2005.
10. Co-chair, Tools and Methodology track, *IEEE Int'l Conf. on Computer Design*, 2004.
11. Program Committee member, *The Great Lakes Symposium on VLSI (GLSVLSI)*, 2004.
12. Program Committee member, *IEEE Int'l. Conf. on Computer Design (ICCD)*, 2003.
13. NSF Review Panel Member, 2002.
14. NSF Review Panel Member 1999.
15. NSF Review Panel Member, 1997.
16. Program Committee member of the *Fault-Tolerant Computing Symp.*, 1997 and 1998.
17. Program Committee member of *Int'l Conf. Parallel Proc.*, 1998.
18. Session Chair at the *International Supercomputing Conf.*, May 1996.
19. Session Chair at the *Scalability Workshop at Int. Parallel Processing Symp.*, April 1993.
20. Member of IEEE Computer Society, ACM, SIGARCH and SIGDA.
21. Reviewed more than 200 papers for various journals like IEEE Trans. on Computers/CAD/PDS/CAS and IEEE/ACM conferences, more than 40 NSF proposals, and a proposal for ESPRC (the U.K. NSF)

Publications

Citations:

A total of around 1050 citations of our papers from the **Google Scholar** site
http://scholar.google.com/advanced_scholar_search. Of these self-citations are at most between 10-15% (based on random sampling of self citation percentage).
Thus around **900 citations** of my papers are from other authors.
Note: Type in "S Dutt" in the author field and choose area "Engineering, Computer Science, and Mathematics". Most of these are my papers (the above counts are only for my papers).

Book Chapters:

1. S. Dutt, F. Rota, F. Trovo and F. Hanchek, "Fault Tolerance in Computer Systems–From Circuits to Algorithms", invited article, in *Electrical Engineering Handbook*, Ed. Wai-Kai Chen, Academic Press, 2004.

2. S. Dutt and D. Boley, "Roundoff Errors", invited article, in Wiley Encyclopedia of Electrical and Electronics Engineering, Prof. John Webster, ed., Vol. 18, 1999, pp. 617-627.

Journals:

1. H. Ren and S. Dutt, "A Provably High-Probability White-Space Satisfaction Algorithm with Good Performance for Standard-Cell Detailed Placement", accepted for publication, *IEEE Trans. VLSI Systems*, to be published June 2010.
   Available at www.ece.uic.edu/~dutt/papers/tvlsi2-09-accepted.pdf

2. S. Dutt and H. Ren. "Discretized Network Flow Techniques for Timing and Wire-Length Driven Incremental Placement with High-Probability White-Space Satisfaction", accepted for publication *IEEE Trans. of VLSI*, to be published June 2010.
   Available at www.ece.uic.edu/~dutt/papers/tvlsi1-09.pdf

3. S. Dutt and L. Li, " Trust-Based Design and Check of FPGA Circuits Using Two-Level Randomized ECC Structures", Special Issue on Security, *ACM Trans. on Reconfigurable Technology and Systems*, 2, 1, Article 6, March 2009, 36 pages.

4. S. Dutt, V. Verma and V. Suthar, "Built-in-Self-Test of FPGAs with Provable Diagnosabilities and High Diagnostic Coverage with Application to On-Line Testing", *IEEE Trans. Computer Aided Design of Integrated Circuits*, Feb. 2008, pp. 309-326.

5. N.R. Mahapatra and S. Dutt, "An efficient delay-optimal distributed termination detection algorithm", *Jour. Parallel and Distr. Computing*, vol. 67, 2007, pp. 1047-1066.

6. N.R. Mahapatra and S. Dutt, "Adaptive Quality Equalizing: High-Performance Load Balancing for Parallel Branch- and-Bound across Applications and Computing Systems", *Jour. of Parallel Computing*, June 2004.

7. S. Dutt, V. Verma and H. Arslan, "A Search-Based Bump-and-Refit Approach to Incremental Routing for ECO Applications in FPGAs", *ACM Trans. Design Automation of Electronic Systems (TODAES)*, 7(4), pp. 664-693, 2002.

8. S. Dutt and W. Deng, "VLSI Circuit Partitioning by Cluster-Removal Using Iterative Improvement Techniques", *ACM Trans. Design Automation of Electronic Systems*, Jan. 2002.

9. N.R. Mahapatra and S. Dutt, "Hardware-Efficient and Highly-Reconfigurable 4- and 2-Track Fault-Tolerant Designs for Mesh-Connected Arrays", *Jour. Parallel and Distr. Computing*, Vol. 61, No. 10, Oct 2001, pp. 1391-1411.

10. N. Mahapatra and S. Dutt, "Random Seeking: A General, Efficient and Informed Randomized Scheme for Dynamic Load Balancing", *Int. Jour. Foundations of Computer Science*, Special Issue on Randomized Computing, Vol. 11 No. 2, 2000, pp. 231-246.

11. S. Dutt and W. Deng, "Probability-Based Approaches to VLSI Circuit Partitioning", *IEEE Trans. CAD*, Vol. 19, No. 5, May 2000, pp. 534-549.

12. S. Dutt, H. Arslan and H. Theny, "Partitioning Using Second-Order Information and Stochastic-Gain Functions", *IEEE Trans. CAD*, Vol. 18, No. 4, April 1999, pp. 421-435.

13. F. Hanchek and S. Dutt, "Methodologies for Tolerating Logic and Interconnect Faults in FPGAs", *IEEE Trans. Computers*, Special Issue on Dependable Computing, Jan. 1998, pp. 15-33.

14. N. R. Mahapatra and S. Dutt, "Sequential and Parallel Branch-and-Bound Search Under Limited-Memory Constraint", *The IMA Volumes in Mathematics and its Applications, Parallel Processing of Discrete Problems*, Vol. 106, Panos, Pardalos (ed), Springer-Verlag New York, Inc. (1998), pp. 139-159.

15. S. Dutt and N.R. Mahapatra, "Node Covering, Error Correcting Codes and Multiprocessors with High Average Fault Tolerance", *IEEE Trans. Comput.*, Sept. 1997, pp. 997-1015.

16. N.R. Mahapatra and S. Dutt, "Scalable global and local hashing strategies for duplicate pruning in parallel A* graph search", *IEEE Trans. Parallel and Distr. Systems*, July 1997, pp. 738-756.

17. S. Dutt and F. Hanchek, "REMOD: A new hardware- and time-efficient methodology for designing fault-tolerant arithmetic circuits", *IEEE Trans. on VLSI Systems*, March 1997, pp. 34-56.

18. S. Dutt and F.T. Assaad, "Mantissa-preserving operations and robust algorithm-based fault tolerance for matrix computations", *IEEE Trans. Comput.*, Vol. 45, No. 4, April 1996, pp. 408-424.

19. N.R. Mahapatra and S. Dutt, "New anticipatory load balancing strategies for scalable parallel best-first search", *American Mathematical Society's DIMACS Series on Discrete Mathematics and Theoretical Computer Science*, Vol. 22, 1995, pp. 197-232.

20. S. Dutt and N.R. Mahapatra, "Scalable load-balancing strategies for parallel A algorithms", Special Issue on Scalability of Parallel Algorithms and Architectures, *Journal of Parallel and Distr. Computing*, Vol. 22, No. 3, Sept. 1994, pp. 488-505.

21. S. Dutt and J.P. Hayes, "A local-sparing design methodology for fault-tolerant multiprocessors", Special Issue on Graph Theory in Computer Science and Other Fields, *Computers and Mathematics with Applications*, Volume 34, Issue 11, Pages 25-50, 1997, Elsevier Science.

22. S. Dutt and J.P. Hayes, "Some practical issues in the design of fault-tolerant multiprocessors", *IEEE Trans. Comput.*, Special Issue on Fault-Tolerant Computing, Vol. 41, May 1992, pp. 588-598.

23. S. Dutt and J.P. Hayes, "Designing fault-tolerant systems using automorphisms", *Journal of Parallel and Distr. Computing*, July 1991, pp. 249-268.

24. S. Dutt and J.P. Hayes, "Subcube allocation in hypercube computers", *IEEE Trans. Comput.*, Vol. 40, March 1991, pp. 341-352.

25. S. Dutt and J.P. Hayes, "On designing and reconfiguring k-fault-tolerant tree architectures", *IEEE Trans. Comput.*, Special issue on Fault-Tolerant Computing, Vol. 39, April 1990, pp. 490-503.

Journal Papers Under Review:

1. H. Ren and S. Dutt, "Effective Power Optimization Under Timing and Voltage-Island Constraints via Simultaneous Vdd, Vth Assignments, Physical Synthesis and Placement" submitted to *IEEE Trans. CAD*, in 2nd round of review.

Refereed Conference Papers Under Review:

1. S. Dutt and H. Ren, "Timing Yield Optimization via Discrete Gate Sizing using Globally-Informed Delay PDF Functions", submitted to *IEEE Int'l Conf. CAD (ICCAD)*, 2010.

Refereed Conferences:

Notes:
(a) Most papers listed below are in conferences with acceptance rates of approximately 20-30%. Papers listed with a ♠ symbol correspond to these conferences. See, for example, http://www.etu.edu.tr/~oergin/acceptance_rates.html for acceptance rate statistics on some conferences.
(b) It is at least as hard to get published in such conferences as in prestigious journals, and these conference publications are considered archival.
(c) Approximate acceptance rates for conferences of papers not listed with a ♠ symbol are given where known. These are generally between 40-50%, and these papers are listed by a ⋆ symbol.

1. ♠-⋆ S. Dutt at al., "Selection of Multiple SNPs in Case-Control Association Study Using a Discretized Network Flow Approach", *Proc. of BICoB 2009*, Springer Lecture Notes in Computer Science , April 2009, pp. 211-223.

2. ♠ H. Ren, and S. Dutt, "Algorithms for Simultaneous Consideration of Multiple Physical Synthesis Transforms for Timing Closure", *Proc. IEEE Int'l Conf. CAD (ICCAD)*, Nov. 2008, pp. 93-100.

3. ♠-⋆ H. Ren, and S. Dutt, "A Network-Flow Based Cell Sizing Algorithm", *17th International Workshop on Logic & Synthesis*, 2008 (regular presentation), pp. 7-14.

4. ♠ H. Ren, and S. Dutt, "Constraint Satisfaction in Incremental Placement with Application to Performance Optimization under Power Constraints", *Proc. IEEE Int'l. Conf. on Computer Design*, 2007, pp. 251-258.

5. ♠ S. Dutt, H. Ren, F. Yuan and V. Suthar, "A Network-Flow Approach to Timing-Driven Incremental Placement for ASICs", , *Proc. IEEE Int'l Conf. CAD (ICCAD)*, Nov. 2006, pp. 375-382.

6. ⋆ F. Rota, S. Krishna and S. Dutt, "Off-Chip Control Flow Checking of On-Chip Processor-Cache Instruction Stream", *Proc. 21'st IEEE Int'l Symp. on Defect and Fault Tolerance in VLSI Systems (DFT)*, Oct. 2006, pp. 507-515 (**acceptance rate 45%**).

7. ♠ V. Suthar and S. Dutt, "Mixed PLB and Interconnect BIST for FPGAs without Fault-Free Assumptions", in *Proc. IEEE VLSI Test Symposium (VTS)*, April 2006, pp. 36-43.

8. ♠ S. Dutt and H. Arslan, "Efficient Timing-Driven Incremental Routing for VLSI Circuits Using DFS and Localized Slack-Satisfaction Computations," *Proc. Design Automation and Test in Europe (DATE)*, March 2006, pp. 768-773.

9. ♠ V. Suthar and S. Dutt, "Efficient On-line Interconnect Testing in FPGAs with Provable Detectability for Multiple Faults", *Proc. Design Automation and Test in Europe (DATE)*, March 2006, pp. 1165-1170.

10. ⋆ V. Suthar and S. Dutt, "High-Diagnosability Online Built-In Self-Test of FPGAs via Iterative Bootstrapping", *Proc. ACM Int'l Great Lakes Symp. on VLSI*, April 2005 (**acceptance rate 40%**).

11. ♠ H. Arslan and S. Dutt, "A Depth-First-Search Controlled Gridless Incremental Routing Algorithm for VLSI Circuits", *Proc. IEEE Int'l. Conf. on Computer Design (ICCD)*, Oct. 2004, pp. 86-92.

12. ♠ V. Verma, S. Dutt and V. Suthar, "Efficient On-Line Testing of FPGAs with Provable Diagnosabilities", *Proc. IEEE/ACM Design Automation Conference*, June 2004, pp. 498-503.
Nominated for a Best Paper Award.

13. ♠ H. Arslan and S. Dutt, "An Effective Hop-Based Detailed Router for FPGAs for Optimizing Track Usage and Circuit Performance", *Proc. ACM Int'l Great Lakes Symp. on VLSI*, April 2004, pp. 208-213.
Note: The acceptance rate for presented papers (the above paper is one) in this conference is $< 30\%$, though the overall rate for all published papers is about 40%.

14. V. Verma and S. Dutt, "Roving Testing Using Built-in-Self-Tester Designs for FPGAs with Effective Diagosability" (poster paper), *ACM Int'l Symp. on Field Programmable Gate Arrays*, Feb. 2004.

15. ♠ H. Arslan and S. Dutt, "ROAD: An Order-Impervious Optimal Detailed Router for FPGAs", *Proc. IEEE Int'l. Conf. on Computer Design*, May 2003, pp. 350-356.

16. F. Trovo, S. Dutt and H. Arslan, "Design and Simulation of an EM-Fault-Tolerant Processor with Micro-Rollback, Control-Flow Checking and ECC", *IEEE APS/URSI International Symposium*, (digest of abstracts), June 2003.

17. ♠ K. Zhong and S. Dutt, "Algorithms for Simultaneous Satisfaction of Multiple Constraints and Objective Optimization in a Placement Flow with Application to Congestion Control", *Proc. Design Automation Conference*, June 2002, pp. 854-859.

18. S. Dutt and H. Arslan, "Evaluation of Processor Faults Due to EM Interference–Concepts and Simulation Environment", *National Radio Science Meeting*, (no proceedings), Jan. 2002.

19. ♠ V. Verma and S. Dutt, "A Search-Based Bump-and-Refit Approach to Incremental Routing for ECO Applications in ", *Proc. IEEE Int. Conf. Comput.-Aided Design*, Nov. 2001, pp. 144-151.

20. ♠ K. Zhong and S. Dutt, "Effective Partition-Driven Placement with Simultaneous Level Processing and Global Net Views", *Proc. IEEE Int. Conf. Comput.-Aided Design*, pp. 254-259, Nov. 2000.

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