ECE 565 — VLSI Design Automation

Fall 2010
MW 2-3:15 pm

Teaching Staff
Instructor: Professor Shantanu Dutt, 355-1314, 930 SEO
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Instructor’s Office Hours: M/W: 3:30-4:30pm

Course web page: http://www.ece.uic.edu/~dutt/courses/ece565/ece565.html
Check this page at least once a week for important messages and announcements.

Course Material
Reference Texts:

Lecture Notes: Some have been posted on the course webpage and others will be handed out in class. It is very important for you to print out the lecture notes on the webpage so that you can follow the class lectures that will mostly use these notes. Most of the class material will be based on these notes which have been derived from the text and sources.

Course Outline
1. VLSI CAD Flow
2. Chip Layout Styles
3. High-Level Synthesis
4. Algorithm Design Approaches for VLSI CAD
5. Brief Exposition of Logic Synthesis and Tech. Mapping
6. VLSI and Circuit Design Issues (power and delay analysis and minimization)
7. Partitioning
8. Floorplanning
9. Placement
10. Global and Detailed Routing

Grading
Tentatively based on: (1) 2-3 homeworks (15%), (2) a midterm exam (20%), (3) a midterm mini paper presentation (10-12 slides, 15 mins)—based on ≥ 3 papers (20%), and (4) a final project, report and presentation (approx. 20-25 slides, 30-40 mins) (45%)

Desired Background
Algorithms (most important—need to have taken or concurrently take CS 401 or equivalent), programming, logic design and VLSI design.