Static Timing Analysis (STA)

Input: DAG $G(V, A)$ with node and/or arc delays.
Output: Critical path delays.

Forward-Trace Process:
1. Let $T$ be the # of levels of $G$ from 0 to $T - 1$, w/ corresponding to inputs.
2. For every input (level-0) node, $(n)p = (n)d_0$, $\forall (n,i)\in V$.
3. For $i$ from 0 to $T - 1$, do:
   - Impacts of level-0 nodes are all assumed to be available at time 0, $n$.
   - $(n)p \leftarrow (n)p + (n)x_{nw}\delta_i$.
   - $(n)\delta_0 = (n)d_0$ [2]
   - $\forall (n,i)\in V$.

max-path delay through every output node $n$.

5. Critical path delay = max $(n)\max_{\forall (n,i)\in V}$ among all output nodes.

4. For every output node $n$ do $(n)d_0 = (n)d_\delta$.

Forward Trace Process:
1. Let $n$ be the # of levels of $G$ from 0 to $T - 1$, w/ corresponding to outputs.
2. For every output node $n$ do $(n)p = (n)d_\delta$.
3. For $i$ from 0 to $T - 1$, do:
   - $(n)p \leftarrow (n)p + (n)x_{nw}\delta_i$.
   - $(n)d_\delta = (n)\delta_0$ [2]
   - $\forall (n,i)\in V$.

max-path delay of every output node.

3. For every input (level-0) node, $(n)p = (n)d_0$, $\forall (n,i)\in V$.
4. For every input (level-0) node, $(n)p = (n)d_0$, $\forall (n,i)\in V$.
5. Critical path delay = max $(n)\max_{\forall (n,i)\in V}$ among all output nodes.

/* would be available (assuming no hardware constraints); */

/* inputs of level-0 nodes are all assumed to be available at time 0 */

/* timing when the output from n */

/* the # of levels from 0 to T */

/* max-path delay through n */

forward-trace analysis (STA)
the largest output delay gives the actual critical path. 10. Tracing back through the \( \text{max-delay} \) from the output node with

\[(n)_{x^{\text{max-delay}}} = (z)do, \text{ s.t. } \begin{cases} \end{cases}, \text{ where } z = \text{(n)max-delay}(q) \text{ \( \text{for-a} \)} \]

\[0 = (n)_{\text{max-delay}}, \text{ for each output node n do} \]

\[\text{Backward Trace Process:} \]

\[\text{Static Timing Analysis (STA) (Cond)}]