ECE 465
Digital Systems

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Lecture Notes # 9

One-Hot Sequential Circuit Implementation
One-Hot Design

- No binary encoding of state
- Each state is implemented by a single and unique FF; generally, a D-FF
- A transition signal (TS) goes from o/p $Q_A$ of FF of state A to i/p OR gate of FF of state B, if there is a transition arc from A to B in the FSM.
- The above TS is generated by AND(i/p condition, $Q_A$). E.g., if in FSM there is a transition from A to B when, say, the 2-bit i/ $x_1x_2 = 01$, then the above TS = AND($x'_1$, $x_2$, $Q_A$).
One-Hot Design (contd)

- Each Mealy FSM output $y_i$ is obtained by OR’ing those TS’s whose corresponding transition in the FSM has a 1 value for the $y_i$ output.
- Each Moore FSM output $z_i$ is obtained by OR’ing the Q o/p s for those FFs that implement states in which $z_i = 1$. 
Example – Simple Vending Machine FSM

- Logic cost = 35 gate i/ps, delay = 6 gate i/p units
- Compare to binary-coded design (Lect. Notes “Seq. Ckt Synth.”) logic cost = 19 gate i/ps, delay = 6 gate i/p units for D-FF impl (less for J-K: 14, 4).
A critical path (max-delay path) in the next-state (NS) logic. Delay is from Q,D,N i/ps to the FF D-ips. Delay = demux delay (3-i/p AND gate delay) + 3-i/p OR gate delay = 6 units

A critical path in the o/p) logic for a Mealy m/c. Delay is from Q,D,N i/ps to the ckt o/p(s). Delay = demux delay (3-i/p AND gate delay) + 3-i/p OR gate delay = 6 units

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Critical path in the o/p) logic for a Moore m/c. Delay is from Q i/ps to ckt o/p(s). Delay = 0 units as there is no logic reqd in this case

(c) One-hot implementation with both Moore & Mealy O/Ps
Advantages (+) and Disadvantages (-)

+ Generally less or comparable logic cost for large designs
+ Generally faster; speed independent of # of states & only dependent on the # of transitions into a state
+ Don’t have to worry about optimal state assignments
+ Easier to design and debug
+ Easier to modify; adding or deleting states or changing excitation functions can be done easily w/o affecting the rest of the machine
- Requires many more FFs. However, overall hardware cost (logic + FFs) is comparable to binary encoded designs.
Appendix – Determining circuit delay

Delays: 2-i/p gates, AND, OR, NAND, NOR: 4ns, XOR, XNOR: 6ns

Determining the max. delay of a circuit:
(1) Path tracing by observation -- prone to human error in large circuits

(2) Recursive formulation: Delay at o/p of gate g_i = \max\{\text{delay of all i/ps to g}_i\} + \text{delay of gate g}_i

Delay of a circuit = \max\{\text{delay at all o/ps}\}