1. Prob. 3.63 using the alternate to Rule 6 (Rule 7) followed by the Sweep-up Phase.  

2. Redo the PIT (covering) part of the 3-function multi-function QM done in class (and given in the notes) using Rule 6 followed by the Replace Phase described below (the example given in the notes does not use Rule 6 strictly; accidently it uses both Rule 6 and 7 in a mix-and-match manner).

   (a) For each row $R_j$ that covers another row, note the subset $\text{Cov}(R_j)$ of rows that it explicitly or implicitly covers (a row $R_i$ is implicitly covered by $R_j$, if $R_i$ is eliminated due to the last of its MTs being eliminated when $R_j$’s inclusion selected and all MTs it covers are eliminated, while $R_i$ is explicitly covered by $R_j$ if $R_i$ is eliminated directly due to the fact that $R_j$ covers $R_i$).

   (b) For each $R_j$ in the final expression, see if any subset of PIs in $\text{Cov}(R_j)$ plus other selected PIs (those in the final expressions) can together cover all MTs of $R_i$. If so, select the min-cost subset $\text{Cov}_{\text{min}}(R_j)$ of $\text{Cov}(R_j)$ that meets this criterion.

   (c) If $\text{cost}(\text{Cov}_{\text{min}}(R_j)) < \text{cost}(R_j)$, then replace $R_j$ by the appropriate PIs in $\text{Cov}_{\text{min}}(R_j)$ in each function expression that $R_j$ occurs in. Note that the cost of each PI $R_i$ in $\text{Cov}_{\text{min}}(R_j)$ is its cost when it was eliminated plus $r - 1$, where $r$ is the number of new (i.e., additional) function expressions $R_i$ is inserted in due to it replacing $R_j$ (possibly along with other PIs in $\text{Cov}_{\text{min}}(R_j)$) in these expressions. $\text{cost}(R_j)$ is its total cost across all expressions it was in before the Replace Phase.

3. Prob. 5.2(b) and (d) from the text. For 5.2(d) use the PAL schematic given in Fig. 5.28 and not Fig. 5.30.

   For the PLA design, use the multi-function QM method using a PI cost of 1 to share as many product terms as possible between the three functions, thereby minimizing the cost of the implementation.

   For the two problems, specify the PLA/PAL size in terms of inputs, outputs and product lines needed for the three functions.

4. (a) Design a 3-bit ripple-carry adder using an appropriate PLA with feedback (using a schematic of the type shown in Fig. 5.14). Specify the PLA size in terms of inputs, total outputs, outputs that feedback to the AND-plane of the PLA, and product lines needed for the design. Obtain the design without using multi-function QM.

   (b) Give clearly stated rationale on whether it is beneficial or not to use multi-function QM for this particular design (Hint: Think of how much product term sharing is possible).

5. Use the divide-and-conquer (D&C) approach to design a combinational multi-bit left-shifting circuit $\text{MUBILS}$ with inputs an $n$-bit number $X$ (the shiftsee) and a $\log_2 n$ bit # $m$ (the shift amount) and outputs a $(2n-1)$-bit number $Z$ that is $X$ shifted $m$ times. E.g., if $X = 11000111$, and $m = 110 = 6$, then $X$ needs to be shifted by 6 bits and $Z = 0110001110000000$. 

   

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ECE 465, Spring 2010, Instructor: Prof. Shantanu Dutt

Homework 3 : Due Mon, March 8
Show the general (for an $n$-bit $X$) D&C breakup of this problem and actually solve the problem for $n = 16$, clearly showing the basic design for shifting $X$ by a 1-bit number (this will be the smallest subproblem at the leaf of your D&C tree) and how two smaller designs are “stitched up” to provide the next larger design, and so forth. **Show all your work in clear and methodical steps.**

**Hint:** Perform the D&C of the design on the shift amount $m$, i.e., the problem is broken up into shifting $X$ by a certain number of bits based on a single bit of $m$ followed by shifting the result based on the rest of the bits of $m$. The latter computation is further broken down in a similar D&C manner.