CS 362 - 12/5/19

Thursday, December 5, 2019 9:34 AM

Final Exam

Tuesday 12/10/19 from 6pm to 8pm

Location based by Last Name

- Last Name: A - H in BSB 140
- Last Name: I - M in LC-C3
- Last Name: N - R in LC-C4
- Last Name: S - Z in LC-C6

From <https://www3.cs.uic.edu/bin/view/CS362/Fall2019>

Info from zyBooks: Chapters 3, 4, 5, 7 and 8

Boolean simplification

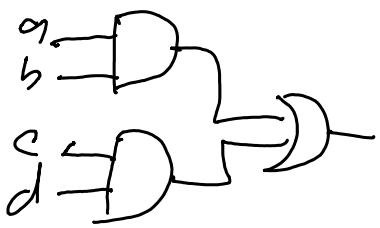
- sum of products (this is most often the target)
- product of sums
- sum of minterms
- don't forget DeMorgan's Law!

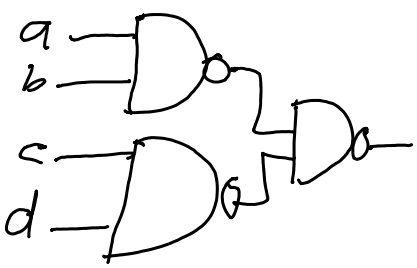
K-Maps

- 3 literals (maybe 4)
- Map Set-up!
- translating from Truth Table (or expression) into Map
- Grouping in set of size of (power of 2)
- use of Don't care conditions

Universal Gates

- only using NAND or NOR gates in a solution
- 2 level gate solution
- NAND gates and NOR actual use less transistors than AND and OR
- See drawing below





Both drawings compute the same circuit

Decoders and Multiplexors
- Use in Datapath (Register file and ALU)
- Rapid Prototyping of Circuits

Register File Make-up/Understanding

Finite State Machines
- Control Unit for the CPU
- State Optimization (redundant state removal)
- States are redundant/duplicated if
    - same output is produced
    - same transition occurs for the same input
- Moore vs Meally Machines
    - Moore: Output is a function of State only
    - Meally: Output is a function of State and input
- FSM to/from Truth Table to/from Equation to/from Circuit

ALU Circuits
- Adder
    - Ripple Carry vs Carry Look-Ahead
- Subtractor
- Comparitor
- Multiplier

Register Operations
- Load Registers
- Clear Registers
- Shift Registers

Speed and Cost of Circuits
Speed - Gate Delays from input to output
Cost - Number of Transistors (2 transistors per gate input)

Memory
- D Flip-Flop - typically used in Registers

- SRAM - typically used in Cache
- DRAM - typically used in Main Memory

Memory Costs
- D Flip-Flop (Cost: 34 transistors)
- SRAM (Cost: 6 transistors)
- DRAM (Cost: 1 transistor and 1 capacitor) (1/5 the density of SRAM)

Memory Speed
- D FlipFlop (registers): gate delays
- SRAM (cache): write - gate delay (for the most part)
  read - sense voltage fluctuation (slow operation)

- DRAM (main memory): write - charge or discharge the capacitor (slower operation)
  read - sense voltage fluctuation
  - "destructive read" requires a write (slowest operation)

- DRAM - capacitors lose voltage stored over time
  - requires "refreshing of the values" - read and write
  - DRAM unit not accessible for 1-2% of time due to refreshing

Arduinos
- wiring question regarding serial communication
- coding question on serial communication
  -see: https://iot-guider.com/arduino/serial-communication-between-two-arduino-boards/
- coding question (more algorithmic)
  - how to use millis() instead of delay()