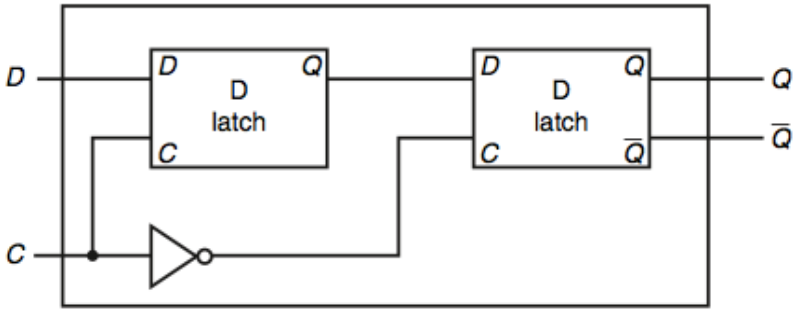
CS 362 Homework 5 NetID: _____

Name: _____

Homework 5: Memory and Finite State Machines

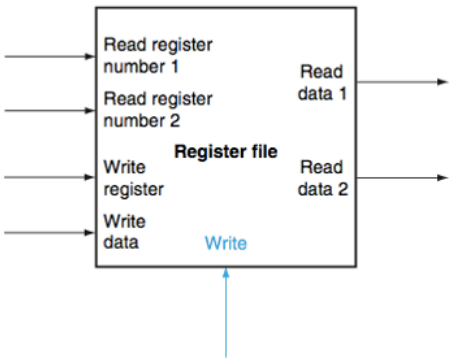
This assignment is to be submitted electronically via Gradescope. You must upload your answers as a PDF to Gradescope by Wednesday, 11/13/19 at 11:59pm.

1. Below is a D-flipflop with a Falling Edge Trigger. Modify it (or redraw the entire diagram) so that it become a D-flipflop with a RISING Edge Trigger. (5 points)



CS 362 Homework 5 NetID: _____

2. (10 points) Below is a high level diagram for a Register File. Assume there are N registers and each regis
ter is holding B bits of data.



Write register: Specifies which register's values gets updated by data on the "Write data" bus when a write operation occurs.

Read register number 1: Specifies which register's values is output via the "Read data 1" bus.

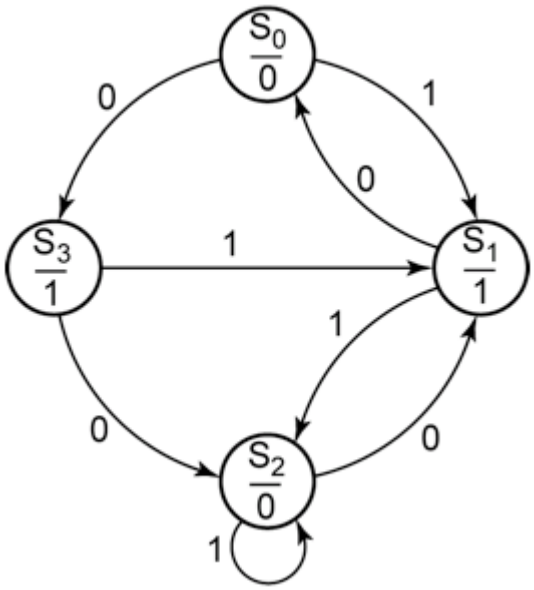
Read register number 2: Specifies which register's values is output via the "Read data 2" bus.

2a. If we wanted to have the ability to write a single value to 2 (or more) registers in the register file, how would the design shown in class have to change? (5 points)

2b. If we wanted to have the ability to write two different values to two different registers in the register file, how would the design shown in class have to change? (5 points)

CS 362 Homework 5 NetID: _____

3. (15 points) Consider the following Finite State Machine.



Start State: S0

Output value is under the line below the State number. i.e.:

S0 outputs a 0

S1 outputs a 1

S2 outputs a 0

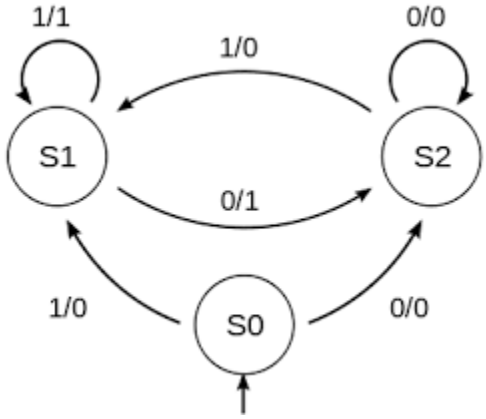
S3 outputs a 1

3a. What is output by the above FSM for the input of: 1 0 1 1 0 0 0 1 0 0 1 1

3b. Create the truth table to the above FSM. Encode the states using 2 bit binary values:
S0 => 0 0, S1 => 0 1, S2 => 1 0, S3 => 1 1

CS 362 Homework 5 NetID: _____

4. (15 points) Consider the following Finite State Machine:



Start State: S0

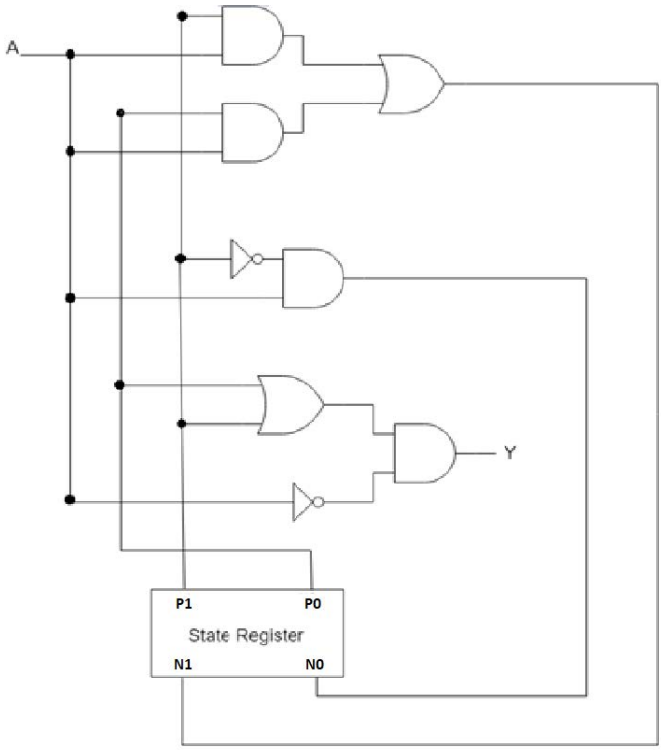
Inputs are listed before the slash on each transition

Outputs are listed after the slash on each transistion

4a. What is output by the above FSM for the input of: 1 0 1 1 0 0 0 1 0 0 1 1

4b. Create the truth table to the above FSM. Encode the states using 2 bit binary values:
S0 => 0 0, S1 => 0 1, S2 => 1 0

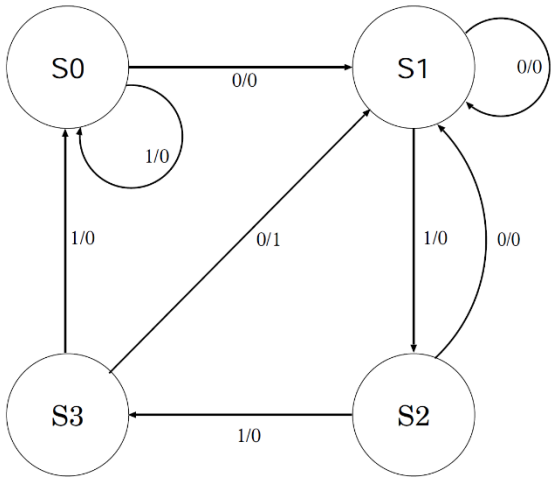
5. (15 points) Consider the following circuit:



5a. Create the truth table for the above circuit:

5b. Draw the Finite State Machine that is represented by the circuit:

6. (20 points) Consider the following Finite State Machine:



Start State: S0

Inputs are listed before the slash on each transistion arc

Outputs are listed after the slash on each transistion arc

6a. Give the truth table for the above Finite State Machine. Encode the states using 2 bit binary values: S0 => 0 0, S1 => 0 1, S2 => 1 0, S3 => 1 1

6b. Design a circuit with equivalent behavior. Use 2 D-flipflops for the memory (which can be shown like the "State Register" in Q. 5). You may use decoders, multiplexors, and/or other gates.

7. (20 points) Suppose we have a machine that takes in an infinite stream of bits, one bit at a time. On every input, the machine will output ’0’, unless the machine has seen the pattern ’10001’ in the last five inputs where it will instead output ’1’. Below is an example of this behavior.

Input: 0100010100010001110010...
Output: 0000010000010001000010...

7a. Design an FSM that exhibits the behavior described above.

7b. Design a circuit with equivalent behavior. Use D-flipflops for the memory (which can be shown similar to the “State Register” in Q. 5). You may use decoders, multiplexors, and/or other gates.