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Noise Analysis and Design Methodologies in Deep Sub-Micron VLSI Circuits

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ABSTRACT

Noise Analysis and Design Methodologies in Deep Sub-Micron VLSI Circuits

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With continuous scaling of VLSI digital circuit technologies, coupling capacitance between interconnect lines is comparable to or even larger than line-to-reference capacitance, and some of the signal lines need more accurate transmission line modeling, requiring the introduction of self and mutual inductances. Consequently, interconnect parasitic elements have become dominant over gate parasitics. These trends, and the increasing usage of dynamic circuits for speed and area requirements, are making signal integrity one of the most critical metrics of performance. Noise can have adverse effects on functional correctness, power, timing, and reliability of CMOS digital circuits.

This work presents an analysis of deep submicron digital integrated circuits in the presence of self and mutual inductances, and illustrates that large error occurs in estimating signal behavior if inductances are neglected. A set of simple closed form expressions are presented to estimate signal behavior, and to intuitively understand some of the characteristics of integrated circuits in the presence of inductances. However, introduction of inductances makes circuit analysis significantly more complex as
compared to circuits without inductances. This work presents an innovative technique for realizable reduction of distributed RLC interconnects circuits including electric (capacitive) and electromagnetic (inductive) coupling. Reduction of extracted netlists is an important step in the performance analysis of deep submicron circuits, since the large amount of data typically generated by extraction tools significantly affect run time and memory issues.

This work also presents closed form analytical solutions for noise as well as noise tolerance metrics for dynamic circuits to analyze the effects of increasing coupling. The analysis of noise in dynamic circuits indicates that noise in dynamic circuits can be made scalable to some degree. Signal deviation caused by noise can lead to functional failure in digital integrated circuits. It has been shown that both static and dynamic digital circuits can suffer logic failure due to noise depending on the switching condition and circuit topology. It is illustrated that increasing frequency may lead to higher probability of noise-driven logic failure due to the possibility of reduced voltage swing at higher frequencies.

Continuous scaling of technologies towards the nanometer range will severely enhance noise and other implications, such as, leakage current levels, contributing to new power consumption sources. These trends are challenging traditional ways of noise avoidance and timing management. Therefore, the presented work must be extended to attempt developing new techniques for better performance in terms of noise immunity, reliability, energy efficiency, speed, and area requirements.
Dedication

My parents:
Dr. M. Anwar Pasha Chowdhury & Hasina Begum Chowdhury

In-Laws:
Dr. Mohammad Faizullah & Nazma Faiz

My Brother:
Sarowar M. Kamal

&

My Wife:
Rizwana Faiz Chowdhury
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Chapter 1: Introduction

Continuous scaling of CMOS technologies, and the increase of circuit complexity are making the role of interconnect in deep submicron digital circuits more prominent [1]-[16], [49]-[53]. Over the last few decades the semiconductor industry exhibited a transition of interconnect modeling from a short circuit to a lumped capacitor to a lossy distributed $RC$ network. However, CMOS technologies now require even more complex modeling of interconnect lines to include the coupling and the magnetic effects in deep submicron integrated circuits [1]-[16], [49]-[53]. Device sizes and interconnect dimensions are being scaled down to provide greater circuit density, resulting in smaller line to ground capacitance. Due to the recent trends of higher aspect ratios and lower spacing between signal lines, the coupling capacitance is becoming comparable to or larger than the line-to-reference capacitance. As a result integrated circuit analysis moved one more step forward to include coupling capacitance between interconnect lines.

Until recently, the inductively induced voltages were generally negligible compared to the effects of the parasitic resistances and capacitances of the interconnect lines. However, with current technology trends, the impact of magnetic fields created by the current flow in a wire can no longer be neglected in terms of its impact on the behavior of high performance integrated circuits. Increasing clock speeds and the desire to push technologies to their ultimate performance limits have made magnetic modeling of ICs one of the most urgent issues for high performance integrated circuit design. The global
nature of magnetic coupling makes inductive effects an extremely challenging modeling and analysis problem. In order to properly deal with this problem, more accurate interconnect modeling and circuit performance characterization are required. Consequently, distributed $RC$ modeling with coupling capacitance between adjacent lines cannot give an accurate picture of the behavior of deep submicron circuits. Both self and mutual inductances need to be included for accurate analysis of current high performance integrated circuits. Factors like smaller feature sizes, increased die area, faster on-chip signal transition time, longer and wider wires, and the push for low resistive materials, are making inductive effects more prominent. Hence, it is imperative to include self and mutual inductances in modeling interconnect lines for high performance VLSI circuit analysis [1]-[16]. Results show that if inductances are neglected in integrated circuit analysis, very large error occurs in estimating signal characteristics such as delay, rise time, overshoots, and wave shapes.

Due to the above transition of current CMOS digital circuit technologies towards distributed $RLC$ models with coupling capacitance and mutual inductance, many commercial and proprietary extraction tools, such as [57], generate $RLC$ circuits for high performance designs. These circuits together with the non-linear drivers are then analyzed by fast timing simulators such as [58] or by interconnect-centric tools such as RICE [59]. Due to the large amount of data typically generated by extraction tools, significant run time and memory issues affect the analysis tools. Therefore, in the past
In recent years, there has been a significant focus on model order reduction methods, which attempt to model the extracted netlist by a smaller model with minimal loss in accuracy. Starting with AWE [60], methods such as [61], [62] use moment matching - either explicitly or implicitly - and projection techniques to generate a low order approximation of the original circuit. More recently, PRIMA [63] modified these techniques to guarantee the passivity of the reduced circuit. Reducing an extracted netlist is an important step before the netlist is fed into tools such as AWE and PRIMA so that they run faster. Since most of the model order reduction methods work with the state-space representation of the circuit and the end result is a set of smaller dimension system matrices, the outputs need to be stamped into analysis tools. In order to take advantage of model order reduction techniques, it is important to have a realizable netlist reduction method, i.e. \( RLC \) in – \( RLC \) out feature. Realizability is important because this avoids the modification of mainstream analysis tools. Circuit reduction techniques based on Gaussian elimination include [66], [68]. A different approach based on Gaussian elimination - called TICER - was presented in [71] for \( RC \) circuits. A method to reduce an \( RLC \) netlist with coupling inductors was presented in [73], but it requires matrix inversion and long runtime. With the current shifts of VLSI technologies to include self and mutual inductances it has become important to develop a realizable method to reduce a netlist with self and mutual inductances. Considering the simplicity and the attractive
features of TICER approach, it would be of great value if this method can be extended to reduce general $RLC$ circuits including mutual inductance.

With the continued scaling in modern deep submicron CMOS processes, noise has become an equally important metric like area, timing, and power dissipation [27]-[30]. To maintain drive strength in the face of scaled down power supply voltages; threshold voltages are also scaled down, resulting in lower noise margins. Among the various sources of noise, crosstalk due to the coupling capacitance and the mutual inductance between interconnect lines, is the dominant source of noise in current CMOS digital integrated circuits. In current CMOS technologies, more levels of interconnect with reduced spacing and higher frequencies are making capacitive and inductive coupling even stronger, leading to severe side effects on signal integrity. When coupling capacitance becomes a first order parameter between two bus lines, two basic signal anomalies can take place. If one line is switching and the other line is steady the energy transfer through the coupling capacitance results in a glitch on the quiet line. The second anomaly, when the two lines are switching in the opposite directions, the result is an increase in signal transition time. When inductance is combined with other elements of the circuit model, the voltage relationship generally results in a higher order differential equation. In addition to glitches and delays, the solution may result in underdamped oscillations, superimposed on top of a glitch or a signal transition [3],[4]. These adverse
effects of coupling noise impose two serious side effects on digital integrated circuits. It can affect timing, which can result in delay failures, and it can cause functional failures.

Performance requirements are driving designs in the direction of using noise-sensitive dynamic circuits. Dynamic logic is gaining popularity for its attractive feature of reduced transistor count with a reduced capacitive load that gives lower area and increased speed for CMOS circuits [28]. Static logic has a major advantage: its superior noise margins. In static circuits, momentary deviation of logic levels can be restored automatically, since at steady state the nodes are always connected either to ground or $V_{dd}$. But this restoration is not possible in dynamic circuits due to the possibility of floating nodes, which makes dynamic circuits very susceptible to noise. If a dynamic node stores its value for a relatively long time, noise currents can discharge the capacitor responsible for holding the logic level at the dynamic node leading to functional failure. Therefore, the analysis of the effects of coupling and other types of noise in dynamic circuits has become very important.

Most of the previous work focused on static noise, and treated noise margins and noise content separately, suggesting that scaling trends are overwhelmingly negative for noise. But it is important to note that noise content itself reduces with the scaling down of supply voltage. Moreover, noise amplitude can be safely higher than static noise margin depending on the length of the operating clock cycle. Consequently, the static noise margins are sometimes conservative measures of noise immunity of dynamic circuits.
Consequently, adhering to the static noise margins could severely restrict the performance of dynamic circuits [36]. Therefore, a more detailed and realistic approach towards noise in dynamic circuits is imperative.

Noise induced errors can cause functional or logic failure in both static and dynamic CMOS digital circuits. The failure modes will be different in different circuit topologies. In current VLSI circuits, where a mixture of static and dynamic implementation is very common, it is important to identify all possible noise failure modes so that designers can adopt methods to prevent these types of functional failures.

Chip designers apply different methods to minimize the effects of various noises, such as, substrate noise, leakage noise, power supply noise, and crosstalk noise. Techniques, like increasing the line width and spacing, buffer insertion, and shielding, etc, are proposed to reduce the effects of capacitive coupling, which is perceived to be the most dominant among the various sources of noise. However, due to the prominence of inductive crosstalk in recent CMOS digital circuits it is important to develop techniques to handle inductive crosstalk together with capacitive crosstalk. Since the usage of dynamic circuits is increasing, it is important to extend all these techniques for dynamic circuits as well as static circuits. To improve noise immunity of digital circuits, various noise tolerant dynamic circuit design techniques have been proposed. But most of the proposed techniques provide improved noise tolerance with the sacrifice of performance and power consumption, which are the most attractive aspects of dynamic circuits.
Chapter 1: Introduction

The rest of the dissertation is organized as follows. Chapter 2 gives the necessary background for the presented research and proposed future continuation of the current work. First the importance of including self and mutual inductances in interconnect modeling is explained. Circuit reduction methods are discussed in the second part of this chapter. Third, the issues of noise and signal integrity in deep submicron CMOS digital integrated circuits are discussed. The fourth section of this chapter discusses the timing performance of deep submicron digital circuits with increasing coupling noise. Merits and demerits of coupling noise reduction methods are discussed in the fifth section. Noise tolerant circuit design techniques are investigated in the last section of this chapter.

In Chapter 3 of this dissertation, a set of simple closed form expressions to estimate VLSI circuit behavior in the presence of self and mutual inductances are presented. These expressions have linear complexity with the number of elements in the interconnect network and an Elmore delay accuracy characteristics. The propagation delay and overshoots estimated based on these formulae are within 15% of AS/X [17] simulations for a wide range of interconnects from IBM’s most recent technology. Besides the use of these expressions in evaluating signal characteristics, the simplicity of the solutions allows intuitive understanding of the behavior of integrated circuits in the presence of self and mutual inductances. Three problems are analyzed based on these solutions. First, a simple figure of merit to determine the importance of inductance in a bus is introduced. Second, the problem of shielding inductance is investigated
analytically and it is shown that inserting ground lines is ineffective in shielding inductance and alternative shielding techniques are discussed. Finally, the delay uncertainty due to different line-switching patterns is investigated. It is shown that inductive coupling always reduces the delay uncertainty (switching window width.)

Chapter 4 presents a realizable reduction method of RLCK circuits (with coupling inductors) by nodal elimination. Since the proposed realizable reduction method is an RLCK-in to RLCK-out, all standard simulators can handle the reduced circuits without any modification. Reduced netlists also guarantee faster simulation and lower memory requirements. It is shown that for an average of 40 to 50% reduction of nodes and elements error in waveform shape calculation is less than 1%. If 3% error is allowed a reduction of about 60 to 70% is obtained. Higher allowance of error results in an even higher reduction. Circuits with mutual inductors are also reducible with the presented algorithm.

In chapter 3 and 4 we have presented the analysis of distributed RLCK circuits with coupling capacitance and mutual inductance. The next few chapters will focus on various signal integrity or noise issues with the growing dominance of coupling capacitance and mutual inductance in distributed RLC interconnect lines.

Due to the increasing popularity of wireless and handheld applications, gradually Systems-on-a-Chip is becoming a reality. Chapter 5 surveys the circuits and signal integrity issues that the designers have to solve to design a complex system on a single
Chapter 1: Introduction

IC. The focus of this chapter is mainly on the physical and circuit level issues like isolation, substrate noise, interconnect coupling, related complexities, and possible solutions for implementing System-on-a-Chip.

Chapter 6 explores the issues of coupling noise in dynamic circuits and proposes a set of analytical expression to analyze noise effects in dynamic circuits. The proposed analytical solutions for noise as well as noise tolerance metrics closely estimate the behavior of a dynamic circuit under the influence of coupling noise. The analytical expressions give results with 5% margin of error with SPICE simulations. It is shown that to some extent, noise can be made scalable with technology due to the linear dependence of noise level on the supply voltage. It is also illustrated that increasing frequency improves noise tolerance by allowing dynamic circuits to tolerate higher noise levels.

Chapter 7 investigates possible logic failure modes in dynamic and static CMOS digital circuits due to signal deviation caused by noise disturbance. Injection of noise causes temporary or permanent signal deviation on a circuit node depending on the level of noise and the affected circuit. The deviation of signal level of the circuit node may lead to functional failure in digital circuits, particularly in dynamic circuit families. Static circuits are inherently robust and can effectively restore the signal deviation before having undesired logic shift. However, some static circuits with a feedback loop cannot recover from noise-induced errors. In current VLSI circuits, where a mixture of static and dynamic implementations is very common, it is important to identify possible noise
failure modes to help designers develop techniques to prevent such failures. It has been observed that a circuit node may suffer from reduced voltage swing at higher frequencies, simply because higher clock rate limits time to fully charge or discharge the load capacitance responsible for holding logic level at a circuit node. At a reduced voltage swing a circuit node is more liable to logic failure due to a certain level of noise. Therefore, this chapter also illustrates the observation that increasing frequency may lead to higher probability of logic failure due to noise.

Future research objectives are presented in Chapter 8. The first section of this chapter briefly explains the delay performance with the growing capacitive and inductive coupling in CMOS digital circuits. The second section presents another scope of future research in power management with increasing problem of noise. This chapter also explains another future research scope to develop techniques to handle both capacitive and inductive coupling in CMOS digital circuits. The next section mentions future possible attempts to develop new noise-tolerant circuit design techniques for better performance in terms of noise immunity, robustness, and reliability together with energy efficiency, speed and area requirements. In addition to the need for fundamental advances in circuit analysis, the explosive growth of integrated circuit complexity calls for a very sophisticated computer-aided design (CAD) approach to system architecture and circuit design. Current research must be extended to create techniques for developing efficient CAD tools for the analysis and design of future integrated circuits.
Finally, Chapter 9 concludes the dissertation by summarizing the presented research results and describing how to extend this research to other related issues of deep submicron CMOS digital circuits.
Chapter 2 : Background

This chapter presents a background of the previous and ongoing work related to the design and analysis of high performance CMOS digital integrated circuits. First, the transitions of interconnect modeling from short circuit to distributed \( RLC \) network with coupling capacitance and mutual inductance is discussed in section 2.1. Due to the complexity in handling extremely large circuit netlists, there has been significant focus on model order reduction methods, which attempt to model the extracted netlists by smaller model with minimal loss in accuracy. A brief survey of the work related to the reduction of a circuit netlists is presented in section 2.2. The third section of this chapter explores noise and signal integrity issues in current CMOS digital integrated circuits. Subsection 2.3.1 explores various sources of noise in deep submicron digital integrated circuits. Considering the growing dominance of coupling among various sources of noise, the impacts capacitive and inductive coupling are briefly studied in subsection 2.3.2. Subsection 2.3.3 emphasizes the fact that signal deviation due to noise may lead to logic failure in both dynamic and static circuits. Section 2.4 explores the effects of growing coupling on the timing performance of deep submicron VLSI circuits. There have been continuous efforts to develop techniques to reduce coupling effects in digital circuits. Section 2.5 of this chapter explores various methods to reduce the effects of capacitive
Chapter 2: Background

and inductive coupling. In the last section of this chapter, a study of noise tolerant circuit design techniques is presented.
2.1 Interconnect Modeling as Distributed RLC Network with Coupling Capacitance and Mutual Inductance

Two decades back, when the minimum feature size was about 5µm, the gate parasitic impedance dominated integrated circuit performance and interconnect lines were modeled as a short circuit. With the continuous scaling of technology, the interconnect capacitance to reference plane became comparable to the gate capacitance, requiring the lines to be modeled as lumped capacitors [42]-[44].

![Diagram](image)

Fig. 2.1 Transition of interconnect modeling from short circuit to distributed $RC$. (a) Short circuit, (b) single lumped capacitor, (c) a lump resistor with a lumped capacitance, and (d) distributed $RC$ line.
With further scaling down of technology, the cross sectional area of the lines has been scaled down to provide more lines per unit area, while the length of the lines has increased. As a result the resistance of long signal lines increased significantly [45], [46]. Consequently, line resistance were required to be included in interconnect modeling as a lumped resistor. Continuous scaling trends pushed interconnect modeling to one more step ahead to distributed $RC$ models for more accurate signal characterization [18], [47]-[54].

As digital technology entered into the era of multi-layer interconnect lines and extremely dense integrated circuits, the line-to-reference capacitance alone has become insufficient for signal behavior analysis. The total capacitance of a line in multi-layer deep submicron digital integrated circuits is now the summation of several components such as (i) line-to-ground capacitance $C_g$, (ii) lateral or coupling capacitance $C_c$ (formed between parallel edges of neighboring lines in the same plane), (iii) parallel or crossover capacitance $C_p$ (due to overlap area of two nets on different layers), and (iv) fringing $C_f$ (formed between the edge of one conductor and the surface of another conductor on different layers) [41]-[44] (see Fig.2.2). The crossover ($C_p$) and fringing capacitances ($C_f$) increase as the number of neighboring metal layers increases around a particular conductor. But, the magnitudes of these two component capacitances are not that significant as compared to other two components of the total capacitance of a line in a multi-layer environment. However, the coupling capacitance to neighboring lines in the
same layer is increasing due to the decrease of spacing between conducting lines, increase of interconnect aspect ratios and increase of length of lines running in parallel in the same layer. Therefore, coupling capacitance has become integral part of interconnect modeling along with line-to-ground capacitance.

![Capacitance in multi-layer representation](image)

Due to faster on-chip rise time and the drive for low resistive lines, currently on-chip inductance have become important. Longer and wider wires in clock distribution networks and upper metal layers exhibit significant inductive effects. Accuracy requirements in deep submicron CMOS technologies, set by these new trends combined
with higher operating frequencies, make it crucial to include self and mutual inductances in the interconnect analysis [1]-[16]. The potential for inductances to become factors of interconnect modeling and analysis of digital integrated circuits, has been increasing. With the current rate of advancement in deep submicron technologies, inductances may become a standard second order factor that designers must trade-off with other performance variables. Consequently, for very complex and high frequency digital integrated circuits, interconnect lines should be modeled as distributed $RLC$ network with coupling capacitance and mutual inductance for better accuracy as illustrated in Fig. 2.3. Fig. 2.3 includes all the factors that influence the behavior of interconnects lines in deep submicron integrated circuits. For the two adjacent lines denoted by $I_1$ and $I_2$, resistances $R_1$ and $R_2$, line-to-ground capacitances $C_1$ and $C_2$, and inductances $L_1$ and $L_2$, and the driver resistance $R_{ON}$ together with the load capacitance will dominate the circuit behavior in submicron domain. However, in deep sub-micron technologies crosstalk due to the coupling capacitance $C_C$ and mutual inductance $M_{12}$ between the two lines is equally important. The degree of crosstalk depends on several factors such as the driver strength $R_{ON}$, line length and width, line spacing, clock speed and skew, driver balance, load-to-load balance, and impedance matching.
There has been a significant amount of work focused on circuits’ performance analysis with distributed $RC$ modeling with coupling capacitance. But self and mutual inductances started drawing attention only in the second half of the last decade. Many publications in last few years explored the issues of inductance, and described criteria to determine which nets should include inductances in analysis [3], [6], [11], [12]. If inductances are neglected very large errors occur for some nets at certain operating conditions. As gate delay decreases due to smaller feature size, the importance of inductance becomes more prominent. With the introduction of self and mutual inductances in interconnect modeling; performance analysis becomes significantly more complex as compared to standard $RC$ modeling. Because magnetic effects have a much longer spatial range than electrostatic effects and a line can be inductively coupled to a large number of lines. Therefore, it is important to include self and mutual inductances in
performance analysis. Considering the complexity of including inductances, a set of simple closed form expressions would be of great importance to quickly estimate the circuit behavior such as propagation delay, oscillations, and overshoots in the presence of self and mutual inductances.
2.2 Reduction of Circuit Netlist for Faster Analysis

Due to the increasing role of interconnect in deep submicron integrated circuits, performing accurate analysis is very important. Current extracted interconnect models contain millions of $RLC$ elements, which far exceeds the simulation capabilities of general purpose simulation tools. Due to the large amount of data typically generated by extraction tools, significant run time and memory issues affect the analysis tools. Therefore, model order reduction has been an area of active research, and in the past decade there has been a significant focus on model order reduction methods which attempt to model the extracted netlist by a smaller model with minimal loss in accuracy. Most of the works that originated from mathematical macro-modeling approaches start with an interconnect model with linear $R$ and $C$ elements and produce reduced order state-space or transfer function representations. These reduced order mathematical macro models often require special non-standard simulator capabilities.

Assymtotic Waveform Evaluation ($AWE$) [60] has been shown to be a very effective method for model order reduction of on-chip interconnect. $AWE$ computes the moments of the original circuit and then matches these moments to a reduced-order transfer function. There has been many effective techniques like $RICE$ [59] to compute the moments by repeated DC solution. But repeated DC solutions for calculating moments have the problem of accuracy loss as the number of moments increases. Besides these
types of model order reduction techniques may result in dense matrices, which can not be
directed realized into passive $RC \ (L)$ elements. This difficulty hinders timing analysis
tools from taking advantage of model order reduction techniques, since timing analysis
tools can only handle lumped circuit models. There have been other techniques [62]-[64]
proposed to increase the accuracy of the model order reduction procedure. Techniques
like $PRIMA$ [63] and [64] modifed the previous techniques to gaurantee passivity of the
reduced-order state equations. However, these techniques do not gaurantee that the
reduced circuit model would be realizable in passive $RLC$ circuits. Realizability is
important because this avoids the modification of mainstream analysis tools to handle
reduced state-space or transfer function representations, since these tools are usually
geread towards reading circuit netlists. Moreover, some analysis tools such as circuit
checkers can only accept inputs in terms of $RLCK$ circuits. Realizable reduction, that has
been largely neglected, is recently drawing attention, e.g., of many [65], [69]-[72].
Realizable circuit reduction approaches include [66]-[68]. A different approach based on
Gaussian elimination - called $TICER$ - was presented in [71] for $RC$ circuits. All the
recent work on realizable reduction focused on $RC$ circuit reduction. With the present
trend of increasing inductive effects [1]-[16], a novel method for realizble $RLC$ circuit
reduction would be of great importance. A method to reduce $RLC$ netlists with coupling
inductors was presented in [73] but it requires matrix inversion and long runtime and is
guaranteed realizable.
The TICER [71] method produces a smaller, realizable, passive RC circuit by selectively removing certain non-port nodes of the original circuit. This method retains the original network topology in the reduced circuit and meets the needs of commercial tools. It keeps designated internal nodes, and preserves dc as well as ac characteristics with the ability to control accuracy. This method defines a time constant for each circuit node, and eliminates nodes with extreme time constants. Consider an $N$-terminal star network (Fig. 2.4), where the central node $N$ is connected to $N$ branches, numbered from 0 to $N-1$, each consisting of a conductance and a capacitance in parallel, denoted by $g_{iN}$ and $c_{iN}$. Some of the elements between node $N$ and $i$ may be absent, and the corresponding term $g_{iN}$ or $c_{iN}$ will be zero. The response of the central node $N$, when a step voltage is applied to the $i^{th}$ terminal, all other terminal being grounded, is given by

$$h_{N} = \frac{g_{iN}}{G_N} + \left( \frac{c_{iN}}{C_N} - \frac{g_{iN}}{G_N} \right) e^{-t/\tau_N}$$

(2.1)

where $G_N = \sum_{k=0}^{N-1} g_{kN}$, $C_N = \sum_{k=0}^{N-1} c_{kN}$, and $\tau_N = \frac{C_N}{G_N}$

(2.2)
The key observation here is that node $N$ responds with characteristics time constant $\tau_N = \frac{C_N}{G_N}$, and this time constant is independent of which neighbor or combination of neighbors is agitated. Therefore, the **time constant of a node**, defined by [71] is the total capacitance from the node to other nodes and to ground divided by the sum of conductances from the node to other nodes and to ground. Depending on the value of the nodal time constants, TICER [71] classifies each node of a circuit into one of the three categories according to whether a node’s time-constant is less than, greater than, or between the min and max time-constants defining the frequency range of interest. The nodes are referred to as **quick**, **slow**, or **normal** according to this criteria. The importance of this classification comes from the fact that both quick and slow nodes can be eliminated from the network without significantly altering its overall behavior in the
frequency range of interest. Now the elimination of node \( N \) results in the addition of a new element between nodes \( i \) and \( j \), whose admittance is given by

\[
y'_{ij} = \left( g_i + sc_i \right) \left( g_j + sc_j \right) / \left( G_N + sC_N \right)
\] (2.3)

According to the described principle node \( N \) will be a candidate node for elimination if one of the following conditions is satisfied.

\[
sC_N << G_N \quad \text{.................. quick node} \quad (2.4)
\]

\[
sC_N >> G_N \quad \text{.................. slow node}
\]

Motivated by the attractive features of TICER method for RC circuits, in one of our previous research results we have extended TICER method to RLC circuits with both inductive and capacitive coupling present. The proposed method eliminates nodes with time constants below a user specified time constant and preserves the dc characteristics and the first two moments at all nodes. It also recognizes and eliminates all the redundant inductances generated by the extraction tools. The proposed method naturally reduces to TICER [71] in the absence of any inductances.
2.3 Noise in Current CMOS Digital Integrated Circuits

Noise can be defined as any deviation of an evaluation node voltage from nominal high or low values as determined by the logic and delay of the circuit in those subintervals of time when it should otherwise be stable [28]. Noise has always been an issue for analog circuits. One of the reasons behind the popularity of digital systems as compared to analog systems was their inherent noise immunity. High gain CMOS static digital circuits can restore any deviation by noise by means of nonlinear voltage characteristics, which significantly reduce noise near high and low voltage rails. However, with the continuous scaling of CMOS digital technologies signal integrity and noise issues have become a metric of comparable importance to area, timing, and power for deep submicron digital integrated circuits. In addition, due to the usage of noise sensitive dynamic circuits, noise issues have become even more important [27]-[40]. Dynamic circuits are more susceptible to noise disturbance because during some part of their operation the evaluation nodes are disconnected from power and ground. Besides static circuits contain both N and P blocks that can be balanced to obtain the highest possible noise margin. This is not the case for dynamic circuits, which have a noise margin as low as the device threshold voltage.

Most of the previous work focuses on static noise. Due to the growing popularity of dynamic circuits it is important to study noise implications in dynamic circuits as well as static circuits. Static noise margins are sometimes conservative for dynamic circuits,
2.3: Noise in Current CMOS Digital Integrated Circuits

because it ignores the fact that logic gates act as low pass filters. Moreover, most of the previous work treated noise content and noise immunity separately. Noise amplitude can safely be higher than the static noise margin depending on the shape of the noise. Both the amplitude and duration of a noise glitch are parameters that determine the extent of noise effects. At higher frequency any noise pulse will have less time to disrupt the nominal logic level, thereby enabling digital circuits to tolerate higher noise level. Therefore, adhering to the static noise margins could severely restrict the performance of the dynamic circuits. Consequently, analysis of noise in dynamic circuits needs a more realistic and detailed approach.
2.3.1 Sources of Noise in Digital Integrated Circuits

Noise sources, that are most relevant to CMOS digital circuits, are (i) charge leakage and substrate noise, (ii) charge sharing noise, (iii) power and ground supply noise, and (iv) coupling or crosstalk noise (see Fig. 2.5) [27], [28], [50]. [108]-[111].

Leakage noise in digital circuits mainly comes from sub threshold conduction due to the off current of FET devices. Bootstrapping causes minority carrier back-injection into the substrate. These currents can either charge or discharge a dynamic node or cause the stable state of a weakly held node to be significantly different from rails. As technology...
2.3.1: Sources of Noise in Digital Integrated Circuits

scales down, the leakage increases exponentially with decreasing thresholds, and is becoming significant from 0.18µm and smaller feature sizes [50]. Moreover, the supply voltage and capacitance of dynamic nodes scale down, reducing the amount of charge stored on the dynamic node.

Charge sharing noise is produced due to the charge redistribution between a weekly held dynamic node and internal nodes of the circuit. The primary technology variable here is the ratio of junction capacitance to gate and interconnect capacitance. For most circuit this noise is not getting significantly worse with new technology generations [50].

Power and ground supply noise refers to noise appearing on the supply and ground nets and coupled onto evaluation nodes through FET conduction path. This noise is measured as the difference between the local voltage references of the driver and receiver, which can appear as a spurious signal to the receiver and cause circuit failure. Power supply noise is a dominant factor in domino circuits.

Crosstalk noise is the voltage induced on a node due to coupling among adjacent nets. Among the various sources of noise coupling or crosstalk is the dominant source of noise in current deep submicron digital integrated circuits. Considering it’s growing dominance as a noise source, coupling is discussed in detail in the next section. There are other noise sources in digital integrated circuits. In highly synchronous logic, large current pulses due to pre-charging and evaluating many nodes simultaneously cause significant $dl/dt$ noise [27]. Process parameters variations, alpha particles, electro-
magnetic radiations, etc, also have substantial impact on the performance of digital circuits as sources of noise.
2.3.2 Coupling or Crosstalk noise

Crosstalk or coupling noise in the noise induced or injected into a victim line due to capacitive and inductive coupling with neighboring lines. Therefore, coupling can be of two types - capacitive and inductive (see Fig. 2.3 and Fig. 2.5). Interconnect cross-capacitance injects charge in quite nets due to the switching of neighboring nets. This is perceived to be the most dominant source of noise in current process technologies [108]-[110].

![Figure 2.6: Increase of lateral capacitance with the decrease of line spacing](image)

Device and interconnect scaling is making the problem worse due to the increasing ratio between coupling to total capacitance. To improve the degrading resistance of long wires, the vertical dimensions of the lines scaled slowly as compared to the horizontal dimension, leading to a very high aspect ratio. At the same time interconnect pitch and spacing came down close to or less than 1µm [50], [53]. Consequently, coupling
capacitance is becoming even stronger due to decreasing spacing, and longer overlap area between lines in the same layer (see Fig. 2.6) [41]-[44], [51]. This is particularly true in the upper metal layers, where power and clock distribution networks, and global signal lines run across the whole chip area. Bus-dominant designs worsen the effects of coupling, since it results in longer parallel runs.

Inductive coupling occurs when signal switching causes transient current to flow through loop formed by the signal wire and current return path, thus creating a changing magnetic field. This induces a voltage on a quiet net. For several switching nets on a wide bus this effect on the quiet wire will be cumulative (see Fig. 2.7, [50]). Faster on-chip rise times in conjunction with wide and synchronous bus structures are making inductive noise significant in current technologies.

![Inductive coupling due to simultaneous switching on a wide bus](image)

Fig. 2.7: Inductive coupling due to simultaneous switching on a wide bus
 Capacitive coupling together with inductive coupling in digital integrated circuits can cause severe noise, which could disturb the proper function of the digital circuit, especially since the supply voltage of those future technology generations will be significantly lower than today. In current CMOS technologies, more levels of interconnect with reduced spacing and higher frequencies are making capacitive and inductive coupling even stronger, leading to severe side effects on signal integrity (see Fig. 2.8).

![Fig. 2.8: Effects of interconnect coupling](image)

When coupling capacitance becomes a first order parameter between two signal lines, two basic signal anomalies can take place. If one line is switching and the other line is steady the energy transfer through the coupling capacitance results in a glitch on the quiet line. The second anomaly, when the two lines are switched in opposite direction, the result is an increase in signal transition time. When inductance is combined with other
elements of the circuit model, the voltage relationship generally results in a higher order differential equation. In addition to glitches and delays, the solution may result in under-damped oscillations, superimposed on top of a glitch or a signal transition. These adverse effects of coupling noise can cause delay failures by causing the effective line capacitance and inductance to increase or decrease in the presence of simultaneously switching coupled lines, increasing or decreasing the signal delay. Second, it can cause functional failures by charging or discharging the capacitor responsible for holding logic level at a dynamic node. In a recent 1 GHz commercial microprocessor, designers had to introduce a 50 MHz reduction in achievable clock frequency due to coupling capacitance effects [74].
2.3.3 Logic Failure due to Noise

A general CMOS circuit has input signals, output signals, internal static and dynamic nodes, and power and ground nodes on which noise can be injected from the various sources. Injection of noise in these various circuit nodes may lead to different kinds of unexpected behaviors including functional failure of digital circuits. Precharged dynamic circuits cannot recover from noise-induced errors, which leads to logic failure. Generally, in static circuit nodes that have a low impedance path to either ground or $V_{dd}$, noise generated by sources other than power or ground is eliminated. However, static latches like $D$ flip-flops have a feedback path that cannot recover from noise-induced errors. Since current CMOS digital designs can have a mixture of dynamic and static implementation in the same circuit, there may be many other possible modes for logic failure. Circuits may change state at some signal switching conditions depending on the incoming noise level, shape, and duration. Since the impact of noise is becoming critical with the scaling trends, it is important to detect all possible modes of logic or functional failure.
2.4 Effects of Increasing Coupling on Timing, Delay Uncertainty and Clock Signal

One of the most harmful effects of noise on circuit operation is the degradation of signal integrity causing uncertainty in the signal delay. The uncertainty of the propagation delay of a signal (that is, the ratio or the gap of the maximum and the minimum signal propagation delay on a signal line) can cause a catastrophic violation of the timing constraints within a system. For capacitively coupled interconnect lines, when neighboring lines switch in the opposite direction, the \( \tau_{RC} \) time constant is maximum due to increased effective capacitance that has to be charged. \( \tau_{RC} \) is minimum when neighboring lines switch in the same direction, since there will be no contribution due to capacitive coupling [54]. Therefore, the gap between the worst and the best signal propagation delay, increases with the increase of capacitive coupling [54], [104]. However, for an inductively coupled system, the \( \tau_{LC} \) time constant decreases when the neighboring lines switch in the opposite direction, since the contributions of inductive coupling between oppositely switching lines are subtractive due to opposite currents in the neighboring lines. The worst-case inductive effects occur when lines are switching in the same direction, since in this case the effect of mutual inductance is additive with the self-inductance [54]. Therefore, increasing inductive coupling tends to decrease the delay uncertainty [54], [105]. This opposite behavior of \( \tau_{RC} \) and \( \tau_{LC} \) results in unpredictable...
discrepancy between the maximum and the minimum signal propagation delays. With the increase of coupling between the high aspect ratio wires, this unpredictability increases in the current design flow.

One of the most critical signals in a synchronous digital circuit is the clock signal. The design of clock distribution networks in synchronous digital systems presents enormous challenges. Controlling the clock signal delay in the presence of various noise sources, process parameter variations, and environmental effects represents a fundamental problem in the design of high-speed synchronous circuits. It is important to reduce the uncertainty of the clock signal delay, particularly of the clock signals driving the registers belonging to the most critical data paths. The delay uncertainty introduced by interconnect coupling in signal lines other than clock signals also imposes additional constraint on the length of clock period. Therefore, the effects of increasing coupling in interconnect networks on the clock period should also be investigated.
2.5 Minimization of Coupling in CMOS Digital Circuits

There have been many techniques proposed to reduce coupling or crosstalk effects in CMOS digital circuits. Widely discussed crosstalk reduction techniques in CMOS digital circuits are increasing lines spacing, widening metal wires, buffer insertion [107], net ordering, shielding, and differential signaling. By increasing line spacing, capacitive coupling can be decreased, but it increases the loop inductance [23]. Widening metal wires helps to decrease the effect of capacitive coupling by increasing the line to ground capacitance, which actually decreases the coupling capacitance to the total capacitance ratio. But increased line to ground capacitance results in increased delay. For very long lines, buffer insertion is required to meet performance requirements. Net ordering techniques [20]-[26] that put sensitive nets apart, are effective for reducing capacitive coupling because these are based on the assumption that coupling is determined mainly by adjacent nets. But this assumption is not correct if inductive coupling is considered due to the long range effects of magnetic coupling [21]-[23].

With increasing device densities, and shrinking device and wire dimensions, wires are becoming longer and more resistive. At the same time clock frequencies are rising. Robust on-chip global signaling in the face of heightened coupling is beginning to place fundamental limits on global clock frequencies. The growing coupling increases the functional amount noise induced on a wire as well as enhances the sensitivity of wire delays to aggressor switching. In a recent 1 GHz commercial microprocessor, designers
found a 50 MHz reduction in achievable clock frequency due to coupling capacitance effects [79]. To reduce the effects of coupling uniform or simultaneous shielding may be used on either or both sides of a signal line[21]-[23], [75]. Shields are ground or power lines placed between two signal wires to prevent direct coupling between them (as illustrated in Fig. 2.9). This shielding methodology used today is passive in that shield wires are tied statically to ground or $V_{dd}$. For coupling between two adjacent lines the worst case is when the two lines are switching in the opposite direction, since the victim line must charge an effective coupling capacitance twice that of nominal one [33], [54], [80]. Again the effective coupling capacitance is zero if the aggressor line switches in the same direction of the victim line. Another shielding approach called active shielding [83], [84] has been proposed to guarantee the best case-case switching scenario for a wire, which is illustrated in Fig.2.10. The concept of active shielding uses shields on either side of the wire that helps speed up signal propagation through the Miller effect. The Miller effect The Miller effect states that the effective coupling capacitance between two nodes is zero if the transitions at the two nodes occur at the same time and in the same direction (a best case scenario can result in a factor of $-1$). However, demand for high density and relatively high cost of wires restricts extensive use of such techniques. A new approach, named clock as shield (CASh) [38], was suggested in which clock lines in domino circuits can be used to shield signal lines from each other to reduce mainly capacitive coupling (see Fig. 2.11). This scheme can save the extra area used by the traditional shielding
methods. But switching clock lines themselves will give rise to another coupling noise on the signal lines. The induced noise voltage due to the switching clock lines may result in functional fault, and nullify the benefit of shielding signal lines by clock lines.

Fig. 2.9: Shielding for minimizing coupling

Fig. 2.10 Active shielding to minimize coupling effects

Fig. 2.11: Clock as shielding for reducing capacitive coupling
All these shielding methods mainly handle capacitive coupling efficiently. However, with growing significance of inductive coupling, it is important to explore the effectiveness of these techniques to handle and reduce the effects of mutual inductance. Since inductive coupling is a long-range phenomenon as opposed to capacitive coupling, a more detailed analysis is required to investigate the effectiveness of the shielding technique to handle inductive coupling. As an improvement over traditional shielding, another technique - called differential signaling, is proposed in [23] to minimize inductive coupling. This scheme exploits differential bus switching for shielding inductance. In this technique, instead of having grounded wire between each pair of signal lines, each signal wire is routed adjacent to its inverse as shown in Fig. 2.12,

![Fig. 2.12. Reduced order Differential bus switching](image)

However, it is important to notice that in this scheme the victim line is always adjacent to its inverse, which contributes worst-case capacitive coupling by switching always in the opposite direction. Therefore, a comparative study is required to investigate these different methods of minimizing capacitive and inductive coupling.
2.6 Noise Tolerant Circuit Design

To improve the noise tolerance of digital circuits, a standard practice is to provide non-precharged feedback latches in dynamic circuits to restore the logic level of evaluation nodes affected by noise. These feedback transistors, known as keeper transistors, are sized so that it will supply enough current to cancel the effects of noise (see Fig. 2.13). But the disadvantages of this technique are ratioed design for the latch transistor, reduced speed, and increased power consumption.

Fig. 2.13: A weak PMOS keeper transistor in feedback loop to prevent output deviation.
One effective way to improve noise immunity is to increase the switching threshold voltage of the gate. Several techniques, such as CMOS inverter technique [39], PMOS pull-up technique [40], and mirror technique [37], have been proposed to improve noise tolerance of domino circuits by increasing the gate switching threshold voltage $V_{tn}$. The CMOS inverter technique (see Fig. 2.14a) modifies the NMOS evaluation net by utilizing static inverters for noisy signal inputs. Clearly the $V_{m}$ of the NAND gate equals the $V_{th}$ of the static inverter, which can be adjusted by tuning the width to length ratio. Noise tolerance is increased if $V_{th}$ is increased above $V_{m}$. However, certain input logic combinations will short $V_{dd}$ to ground for dynamic OR/NOR logic. The PMOS pull-up technique (see Fig. 2.14b) utilizes a pull-up device to provide biased voltage in dynamic evaluation net. This technique increases $V_{th}$ during the evaluation phase. But this technique suffers from increased static power dissipation, and is not suitable for low power applications. The mirror technique (see Fig. 2.14c) uses an extra NMOS evaluation net and a transistor $M$ to increase the switching threshold of the gate. It guarantees zero static power dissipation, but suffers from higher area penalty than previous two techniques. There can be a speed penalty too if the devices are not resized.
Fig. 2.14: Noise tolerant domino NAND gate design techniques. (a) CMOS inverter technique, (b) PMOS pull-up technique, and (c) Mirror technique.
Chapter 3 : Behavior and Analysis of Deep Sub-micron Integrated Circuits Including Self and Mutual Inductances

This chapter introduces Elmore-like closed form solutions to analyze the behavior of integrated circuits in the presence of self and mutual inductances. These expressions have linear complexity with the number of elements in the interconnect network and an Elmore delay accuracy characteristics. The propagation delay and overshoots estimated based on these formulae are within 15% from AS/X simulations for a wide range of interconnects from IBM’s most recent technology.

Besides the use of these expressions in evaluating signal characteristics, the simplicity of the solutions allows intuitive understanding of the behavior of integrated circuits in the presence of self and mutual inductances. Three problems are analyzed based on these solutions. First, a simple figure of merit to determine the importance of inductance in a bus is introduced. Second, the problem of shielding inductive coupling is investigated analytically and it is shown that inserting ground lines is ineffective in shielding inductive coupling, and alternative shielding techniques are discussed. Finally, the delay uncertainty due to different line-switching patterns is investigated. It is shown that inductive coupling always reduces the delay uncertainty (switching window width).
3.1 Introduction

In current deep sub-micrometer CMOS technologies interconnect parasitic elements are dominating factors of integrated circuits’ performance [1]-[16]. Recent CMOS technologies using low resistance metals for interconnects such as copper [49],[6] and higher operating frequencies make it crucial to include the self and mutual inductances in the interconnect model. For example, three sets of AS/X [17] simulation results are presented based on IBM’s most recent technology to illustrate the importance of on-chip self and mutual inductances. The first example is a 4-bit coupled bus (see Table 3.1). The second example is a tree coupled with two lines (see Table 3.2). And the third example is a pair of lines coupled with each other (see Table 3.3). In all three examples simulations are done for three cases. In case-I, self and mutual inductances are not included. That is, signal lines are considered as standard $RC$ lines with coupling capacitances only. In case-II, self-inductance is included, and lines are considered as $RLC$ lines with coupling capacitance, but no coupling inductance. In case-III, both self and mutual inductances are included and lines are considered as $RLC$ lines with coupling capacitance and mutual inductance. Results show that the error due to neglecting inductance can be more than 100% for the delay calculation and 70% in the rise time. Hence, it is imperative to include self and mutual inductances in the interconnect modeling for proper fault free VLSI circuit analysis [2]-[5], [9]-[12].
Table 3.1: AS/X simulation of a 4-bit BUS.

<table>
<thead>
<tr>
<th>BUS</th>
<th>Case</th>
<th>Delay (ns)</th>
<th>Rise Time (ns)</th>
<th>% Overshoot (%)</th>
<th>Time of overshoot (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I</td>
<td>II</td>
<td>III</td>
<td>I-III</td>
<td>II-III</td>
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<td>44.2</td>
<td>58.67</td>
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<td></td>
<td>-</td>
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<td>155.2</td>
<td>-</td>
<td>35.3</td>
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</table>

Table 3.2: AS/X simulation of a coupled tree network

<table>
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<tr>
<th>TREE</th>
<th>Case</th>
<th>Delay (ns)</th>
<th>Rise Time (ns)</th>
<th>% Overshoot (%)</th>
<th>Time of overshoot (ns)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>III</td>
<td>I-III</td>
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<td>-</td>
<td>18.2</td>
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</tbody>
</table>

Table 3.3: AS/X simulation of a pair of coupled lines

<table>
<thead>
<tr>
<th>LINE</th>
<th>Case</th>
<th>Delay (ns)</th>
<th>Rise Time (ns)</th>
<th>% Overshoot (%)</th>
<th>Time of overshoot (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I</td>
<td>II</td>
<td>III</td>
<td>I-III</td>
<td>II-III</td>
</tr>
<tr>
<td></td>
<td>63.12</td>
<td>74.13</td>
<td>83.64</td>
<td>32.53</td>
<td>12.83</td>
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<td>67</td>
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<td>0</td>
<td>0.74</td>
<td>6.2</td>
<td>-</td>
<td>737</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>269</td>
<td>221.5</td>
<td>-</td>
<td>17.69</td>
</tr>
</tbody>
</table>

With the introduction of self and mutual inductances in modeling interconnect lines, performance analysis becomes significantly more complex as compared to standard RC modeling [2]-[5], [9]-[12]. This complexity is aggravated by the fact that a line can
inductively couple to a large number of lines. To quickly estimate the circuit behavior such as propagation delay, oscillations, and overshoots in the presence of self and mutual inductances, a set of simple closed form expressions would be of great importance.

![Fig. 3.1. Signal behavior on one net of a 4-bit BUS](image)

The rest of the chapter is organized as follows. A set of closed form expressions, which can handle inductively and capacitively coupled trees are introduced in section 3.2. The complexity of these expressions is linear with the number of elements in the interconnect network, and has Elmore delay accuracy characteristics [5]. Section 3.3 illustrates some applications of the models developed in this chapter regarding the importance of inductance in busses, shielding inductive coupling, and delay uncertainty.
3.1: Introduction

Conclusions are provided in section 3.4 and the derivation of the moments of inductively and capacitively coupled trees are presented in the appendix A.
3.2 Closed Form Expressions in the Presence of Self and Mutual Inductances

Elmore and Wyatt [18],[19] delay models do not properly characterize RLC networks due to the possibility of a non-monotone response of RLC network. To illustrate this point, consider the simple RLC branch as shown in Fig.3.2, which has a second order transfer function that can be characterized by

\[ g(s) = \frac{1}{s^2 LC + sRC + 1} \]  \hspace{1cm} (3.1)

\[ \text{Fig.3.2 Simple RLC branch} \]

Note that the coefficient of \( s \) is \( RC \), which is the coefficient of Elmore and Wyatt time constant, and it does not depend on the inductance \( L \). However, inductance can have significant effects on the response of the circuit. To better observe the effects of inductance on signal characteristics such as delay and overshoots, a second order approximation as in (3.2) [5] can be made for the transfer function at any node of a capacitively and inductively coupled RLC interconnect.
3.2: Closed Form Expressions in the Presence of Self and Mutual Inductances

\[ g(s) = \frac{\omega_n^2}{s^2 + s2\zeta\omega_n + \omega_n^2} \]  

(3.2)

The transfer function in (3.2) can be expanded in powers of \( s \) as,

\[ g(s) = 1 - s\left(\frac{2\zeta}{\omega_n}\right) + s^2\left(-1 + \left(\frac{2\zeta}{\omega_n}\right)^2\right) - \ldots = 1 + m_1s + m_2s^2 + \ldots \]  

(3.3)

where the first two moments of the transfer function are equated to the first two moments of the system, \( m_1 \) and \( m_2 \). Hence, the parameters that characterize the second order approximation (damping factor \( \zeta \) and natural frequency \( \omega_n \)) can be calculated in terms of the first two moments of the system as given by

\[ \zeta = -\frac{m_1}{2} \frac{1}{\sqrt{m_1^2 - m_2}} \quad \text{and} \quad \omega_n = \frac{1}{\sqrt{m_1^2 - m_2}} \]  

(3.4)

To calculate \( \zeta \) and \( \omega_n \), the first and second moments of the system need to be calculated. It is shown in the appendix A that the first and the second moments of the transfer function at node \( i \) of a set of inductively and capacitively coupled trees are given by expressions (3.5) and (3.6) for step input, respectively. See the appendix A for the detailed derivation of these formulae.

\[ m_{1,i} = -\sum_k \left[ R_k \cdot \sum_{r,j} C_{ij} \cdot (\alpha_r - \alpha_j) \right] \]  

(3.5)

\[ m_{2,j} = -\sum_k \left[ R_k \cdot \sum_{r,j} C_{ij} \cdot (m_{1,r} - m_{1,j}) \right] - \sum_k \left[ L_k \cdot \sum_{r,j} C_{ij} \cdot (\alpha_r - \alpha_j) + M_k \cdot \sum_{i,m} C_{im} \cdot (\alpha_i - \alpha_m) \right] \]  

(3.6)
where \( k \) runs over all the branches on the path from the primary input to node \( i \) on the tree, which \( i \) belongs to; \( r \) runs over all the nodes downstream of \( k \) on that tree, and \( j \) runs over all the nodes to which \( r \) has a capacitance connected to. In the case of capacitances to ground, \( j = 0 \). The index \( l \) runs over all the nodes downstream of \( M_i \) on the coupled tree (which \( i \) does not belong to). The index \( m \) runs over all the nodes which \( l \) has a capacitance connected to. See the appendix for an example of how to calculate these expressions.

Each line has a switching factor associated with it and is denoted \( \alpha_i \) for interconnect \( i \). The switching factor takes the values 1, 0, and \(-1\) for lines switching from low-to-high, non-switching lines, and lines switching from high-to-low, respectively. Substituting the moments of (3.5) and (3.6) in (3.4), the expressions in (3.7) for the damping factor and natural frequency result, where \( \tau_{RC} \) and \( \tau_{LC} \) are given by (3.8) and (3.9), respectively. These formulae are simple, recursive, and can be calculated in linear time with the number of elements in the network.

\[
\zeta = \frac{1}{2} \frac{\tau_{RC}}{\tau_{LC}} \quad \text{and} \quad \omega_n = \frac{1}{\tau_{LC}},
\]

(3.7)

\[
\tau_{RC} = \sum_k \left[ R_k \cdot \sum_{r,j} C_{rj} \cdot (\alpha_r - \alpha_j) \right]
\]

(3.8)

\[
\tau_{LC} = \sqrt{\sum_k \left[ L_k \cdot \sum_{r,j} C_{rj} \cdot (\alpha_r - \alpha_j) + M_k \cdot \sum_{l,m} C_{lm} \cdot (\alpha_l - \alpha_m) \right]}
\]

(3.9)

Note that the approximation that \((m_{1,i})^2\) is equal to the first term of \(m_{2,i}\) has been used. This
same approximation is used in Elmore and Wyatt delay models [18],[19] and in the equivalent Elmore delay model [5], and is particularly accurate in the case of balanced interconnect structures as explained in [5]. Once the damping factor and natural frequency are determined at a certain node for an arbitrary switching pattern, the propagation delay, and the percentage overshoots can be determined for step inputs as described in [5]. The expressions for propagation delay and percentage overshoots are given by (3.10) and (3.11), respectively, where $t_{pdi}$ is the propagation delay at node $i$ and $%O_i$ represents the maximum overshoots due to oscillation for $n$ odd and minimum undershoots for $n$ even at node $i$.

$$ t_{pdi} = (1.047e^{-\frac{\xi}{0.35}} + 1.39\xi_i) / \omega_n $$

$$ %O_i = (-1)^{n+1} \cdot 100 \exp\left(-\frac{n\pi\xi_i}{\sqrt{1-\xi_i^2}}\right) \quad n = 1, 2, \ldots $$

Table 3.4: Delay—simulation vs. approximation

<table>
<thead>
<tr>
<th>Case</th>
<th>BUS</th>
<th>Tree</th>
<th>Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Simulation</td>
<td>29.32</td>
<td>30.46</td>
</tr>
<tr>
<td></td>
<td>Approximation</td>
<td>31.64</td>
<td>29.20</td>
</tr>
<tr>
<td></td>
<td>Margin of error</td>
<td>7.9%</td>
<td>4.14%</td>
</tr>
<tr>
<td>II</td>
<td>Simulation</td>
<td>44.14</td>
<td>43.59</td>
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<tr>
<td></td>
<td>Approximation</td>
<td>41.06</td>
<td>45.02</td>
</tr>
<tr>
<td></td>
<td>Margin of error</td>
<td>7%</td>
<td>3.28%</td>
</tr>
<tr>
<td>III</td>
<td>Simulation</td>
<td>58.67</td>
<td>51.98</td>
</tr>
<tr>
<td></td>
<td>Approximation</td>
<td>50.8</td>
<td>51.00</td>
</tr>
<tr>
<td></td>
<td>Margin of error</td>
<td>13%</td>
<td>1.89%</td>
</tr>
</tbody>
</table>
Table 3.5: %overshoot– simulation vs. approximation

<table>
<thead>
<tr>
<th>Case</th>
<th>Simulation</th>
<th>BUS</th>
<th>Tree</th>
<th>Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>III</td>
<td>Simulation</td>
<td>23.80</td>
<td>15</td>
<td>6.2</td>
</tr>
<tr>
<td></td>
<td>Approximation</td>
<td>27.36</td>
<td>13.56</td>
<td>5.45</td>
</tr>
<tr>
<td></td>
<td>Error</td>
<td>15%</td>
<td>10%</td>
<td>12%</td>
</tr>
</tbody>
</table>

Table 3.4 compares the delay from AS/X simulations with the delay values calculated by the approximate expressions. In almost all the cases the delay formula estimates the propagation delay within less than 10% margin of error. Table 3.5 presents a comparison for the percentage maximum overshoot. The overshoot formula estimates percentage maximum overshoot closely for all the three examples, for the case when lines are modeled as distributed \( RLC \) with capacitive and inductive coupling. The error in this case is within 15%.

![Diagram of coupled transmission lines](Image)

Fig. 3.3. 5 identical uniform equidistant coupled transmission lines
Close observation of the expression for $\tau_{LC}$ (3.9) reveals that switching directions of the lines may lead to a negative term under the square root in the expression (3.9). For example let us consider the five equidistant uniform coupled transmission lines of Fig. 3.3. Here line 1 is capacitively coupled with only adjacent lines (lines 2 and 4), but it is inductively coupled with all lines (lines 2, 3, 4 and 5).

When line 1 is switching in the opposite direction of all other lines the expression for $\tau_{LC}$ at the end of line 1 becomes

$$2\tau_{LC}^2 = \frac{L_T C_T}{2} + \frac{2L_T C_{CT}}{2} - \frac{M_T C_T}{2} + \frac{2M_T C_{CT}}{2} - \frac{M'T C_T}{2}$$

(3.12)

$L_T$ is the total self-inductance of each line; the total line to ground capacitance ($C_T$) of one line equals the total coupling capacitance between two adjacent lines ($C_{CT}$). The total mutual inductance $M_T$ between two adjacent lines (1 and 2 or 1 and 4) equals two times the total mutual inductance $M'T$ between two non-adjacent lines (lines 1 and 5 or lines 1 and 3). With the above simplifications ($M'T = 0.5M_T$ and $C_T = C_{CT}$) the expression for $\tau_{LC}^2$ can be written as:

$$\tau_{LC}^2 = 2.5L_T C_T - 3.5M_T C_T$$

(3.13)

Now for $\tau_{LC}$ to be negative:

$$2.5L_T C_T - 3.5M_T C_T \leq 0 \quad \text{or} \quad M_T \geq 0.7L_T$$

(3.14)

The coupling coefficient between two inductively coupled lines is given by
Since the lines in the above example are identical (L1 = L2)

\[ K = \frac{M_{12}}{\sqrt{L_1 L_2}} \]  

(3.15)

Therefore the critical values of coupling coefficient for the above example circuit for \( \tau_{LC} \) to become negative are \( K \geq 0.71 \) and \( K' \geq 0.355 \).

\[ K = \frac{M_r}{L_r} \quad \text{and} \quad K' = \frac{M_{r'}}{L_{r'}} \]  

(3.16)

Fig. 3.4. Voltage at the end of line 1 (i) \( K = 0.4 \) and \( K' = 0.2 \); (ii) \( K = 0.6 \) and \( K' = 0.3 \); and (iii) \( K = 0.71 \) and \( K' = 0.355 \)

Any value of coupling coefficient equal to or above the critical value is not physically possible, since at the critical point and above, the overall effective impedance of the line under consideration becomes negative and the interconnect circuit becomes unstable, which is not possible for a passive structure. The simulation results (Fig. 3.4) show that
as the value of coupling coefficient becomes closer to the critical value the circuit’s behavior deviates more from it’s stable state due to the overall effective negative impedance of line 1. For different circuits these critical values will be different, but for any particular circuit it is not physically possible to have coupling coefficients equal to or greater than these values as illustrated by the above simulation results. Therefore, a negative term under square root in the expression for $\tau_{LC}$ is nonphysical.
3.3 Some Applications of the Delay Model

Besides the use of the model introduced here for estimating the signal behavior, the model can be used for several other applications due to its simple and closed form nature. Three examples are illustrated in this section. In subsection A, the role of the damping factor as a figure of merit in determining inductive effects is discussed. The effectiveness of inductive shielding techniques are discussed based on the approximations in subsection B and it is shown that inserting ground lines is almost ineffective in shielding inductance. Subsection C discusses the effects of inductance and inductive coupling on delay uncertainty and it is shown that increasing inductance effects results in decreasing the delay uncertainty.

A. Damping Factor as a Figure of Merit

The poles of the second order transfer function (3.2) can be given by the following expression

\[ P_{1,2} = \omega_n \left[-\zeta \pm \sqrt{\zeta^2 - 1}\right]. \]  

(3.17)

When the value of damping factor \( \zeta \) becomes less than one, the poles of the second order transfer function become complex. In that case, the response is under damped and oscillations and overshoots are observed in the response due to inductance effects. If \( \zeta \) is greater than one, the poles are real and the response is over damped. If \( \zeta \) is equal to one, the
response is said to be critically damped. Hence, this direct correlation between the damping factor and inductance effects suggests the use of the damping factor as a figure of merit for characterizing inductance effects.

![N-bit bus diagram](image)

**Fig. 3.5.** N-bit bus, lines are switching in the same direction.

The value of $\zeta$ is given by (3.7) and depends on the $\tau_{RC}$ and $\tau_{LC}$ time constants given by (3.8) and (3.9), respectively. For the important special case of an N bit bus shown in Fig. 3.5, when all the lines are switching in the same direction (resulting in worst case inductance effects), the expressions (3.8) and (3.9) for $\tau_{RC}$ and $\tau_{LC}$ in a particular line $p$ can be expressed as in (3.18) and (3.19), respectively. Line $p$ is inductively and capacitively coupled with all other signal lines in the bus.

\[
\tau_{RC} = \frac{R_{Tp} \cdot C_{Tp}}{2} \quad (3.18)
\]

\[
\tau_{LC}^2 = \frac{L_{Tp} \cdot C_{Tp}}{2} + \sum_{k=1, k\neq p}^{N} \frac{M_{Tpk} \cdot C_{Tk}}{2} \quad (3.19)
\]

where $R_{Tp}$, $L_{Tp}$, and $C_{Tp}$, are the total resistance, inductance and line to ground capacitance of the $p^{th}$ line, respectively. $M_{Tpk}$ is the total mutual inductance between lines $p$ and $k$. If all the lines of the bus are identical then the damping factor is given by
\[ \zeta = \frac{R_{TP}}{2} \sqrt{\frac{C_{tp}}{L_{TP} + \sum_{k=1}^{N} M_{TPk}}} \]  

(3.20)

Since the lines are switching in the same direction, the coupling capacitances have no effect on \( \tau_{RC} \) and \( \tau_{LC} \). Note that the inductive coupling directly adds to the self-inductance when all the lines are switching in the same direction and that the collective effect of inductive coupling can be significantly higher than the self-inductance in this case. To test the validity of these expressions, the signal behavior on a line coupled with two other lines is investigated with different levels of inductance and inductive coupling. Each time \( \zeta \) is calculated according to (14) and AS/X simulations are performed. As shown in [3] the damping factor correctly predicts the amount of inductance effects in the bus. Smaller \( \zeta \) (as compared to one) indicates higher inductance effects and vice versa.

Fig. 3.6 Circuit behavior with changing \( \zeta \)
B. Effectiveness of Shielding in the Presence of Inductive Coupling

In this section, the effectiveness of shielding schemes in the presence of inductive coupling is examined. To minimizing the effects inductive coupling, it is required to minimize the $LC$ time constant given by (3.19) as compared to the $RC$ time constant in the worst case when all the lines switch in the same direction. This objective is equivalent to making the damping factor $\zeta$ high in the worst case.

One of the most commonly used techniques to reduce coupling noise is to insert ground or power lines in between signal lines [20]-[23],[75]. For example, if one shielding wire $g$ is inserted in the above bus example as in Fig. 3.7, the shield line will introduce some positive and negative terms in the expressions (3.18) and (3.19) due to it’s coupling with all the signal lines in the bus.

![Fig. 3.7. N bit bus with a shield wire $g$. Current in the shield wire is in the opposite direction of that in the signal lines.](image)
Since the shielding wire is grounded, there will be a contribution due to the coupling capacitance between the shielding wire and any other signal line. In the presence of a shielding wire, expressions (3.18) and (3.19) are modified as follows

$$\tau_{RC} = \frac{R_T \cdot (C_{T_p} + C_{C_T \rho_C})}{2}. \quad (3.21)$$

$$\tau_{LC}^2 = \frac{L_{T_p} \cdot (C_{T_p} + C_{C_T \rho_C})}{2} + \sum_{k=1}^{N} \frac{M_{T_p k} \cdot C_{T_k}}{2} + \sum_{k=1}^{N} \frac{M_{T_p k} \cdot C_{g_k}}{2} - \sum_{k=1}^{N} \frac{M_{T_g k} \cdot C_{C_T \rho_g}}{2}. \quad (3.22)$$

The negative term in (3.22) is due to inductive and capacitive coupling between the shielding wire and all other lines, which causes negative currents in the ground line. However, note that other positive terms appear in the $LC$ time constant due to the extra positive currents in the signal lines resulting from the extra coupling capacitance to the ground line (shield) that now has to be charged. In the case when all the lines are switching in the same direction (and no shield was present), these currents were nonexistent. Hence, it is not very effective to reduce the $LC$ time constant in the worst case by adding a grounded shield. Therefore, traditional shielding is partially able to shield inductive coupling.

Recently another scheme exploiting differential bus switching was suggested in [23] for shielding inductance and appears to be effective according to our model. In this technique, instead of having grounded wire between each pair of signal lines, each signal
wire is routed adjacent to its inverse as shown in Fig. 2.12. In that case the $LC$ time constant is given by

\[
\tau = \frac{L_{T_{p+1}}}{2} (C_{T_{p+1}} + 2C_{T(p+1)p}) + \frac{M_{T(p+1)p}}{2} (C_{T_q} + 2C_{T_{pq}}) + \frac{M_{T(p+1)p}}{2} (C_{T_p} + 2C_{T_{pq}} + 2C_{T(p+1)p}) \tag{3.23}
\]

![Fig. 3.8. Reduced order Differential bus switching](image)

The above formula assumes that line $p$ switches in the opposite direction of $q$ and $p+1$. Hence, the negative term is much more higher than the negative term in (3.22). As a result, reduction of inductive coupling effects by this scheme will be significant. The intuitive reasoning behind this scheme is that there is as much total positive current as negative current which makes each pair of opposite switching lines appear as almost zero current for other lines. However, it should be mentioned that this technique severely impacts the total power consumed by the bus increasing it several folds as compared to the case of no shielding and multiplies the bus area by two. Hence, there is a significant price for shielding inductive coupling.
C. Inductive Effects and Delay Uncertainty

The ratio of the maximum and the minimum signal propagation delay on a signal line can be defined as delay uncertainty $D_U$ as in (3.24).

$$D_U = \frac{t_{d_{\text{max}}}}{t_{d_{\text{min}}}}$$  \hspace{1cm} (3.24)

Now for a set inductively and capacitively coupled $RLC$ lines, the delay is given by

$$t_d = 1.047 \cdot E \cdot \tau_{LC} + 1 \cdot 4 \cdot \tau_{RC}$$  \hspace{1cm} (3.25)

Here $E$ is the term containing the exponent of $\zeta$ in (3.10). The two time constants $\tau_{RC}$ and $\tau_{LC}$ depend on the switching directions of the neighboring lines. When neighboring lines switch in the opposite direction of the line under consideration, $\tau_{RC}$ is the maximum due to increased effective capacitance that has to be charged. $\tau_{RC}$ (given by (3.8)) is the minimum when all the lines switch in the same direction, since there will be no contribution due to capacitive coupling. However, $\tau_{LC}$ decreases when the neighboring lines switch in the opposite direction, since the contribution due to inductive coupling is subtractive in (3.9) due to the opposite currents in the neighboring lines. The worst-case inductive effects occur when lines are switching in the same direction, since in this case the effect of mutual inductance is additive with the self-inductance as in (3.19). This opposite behavior of $\tau_{RC}$ and $\tau_{LC}$ results in reducing the discrepancy between the maximum and the minimum delays of a line due to coupling with other lines.
AS/X simulation (Fig. 3.9) for the signal on the middle line of three coupled lines shows that as inductive effects increase, the ratio between the maximum and the minimum delays decreases. That is, higher inductive effects lead to lower delay uncertainty and narrower switching windows. Lowering delay uncertainty is a positive effect of inductance since narrower switching windows gives significant degrees of freedom in physical design to limit noise and control glitches among many other benefits.

![Fig. 3.9. Delay Uncertainty](image-url)
3.4 Conclusion

It is shown in this chapter that in analyzing VLSI circuit if standard distributed $RC$ models are used ignoring inductive effects, large errors occur in the prediction and evaluation of the circuit behavior. It is observed that the self and mutual inductances affect deep sub-micron VLSI circuit performance by increasing signal propagation delay and oscillations, and decreasing rise time at any given input switching condition. The closed form expressions presented here gives results fairly close to simulation data (within 15% of AS/X) and can be evaluated in a time comparable to Elmore delay. The model can be used as figure of merit to characterize the importance of self and mutual inductances. With the increase of inductive effect the value of damping factor decreases, resulting in higher oscillations and delay due to higher inductance effects. On the basis of the approximations it is analytically shown that ground shielding is not effective in minimizing coupling in the presence of inductive effects, and differential bus switching scheme can give better coupling minimization as compared to traditional shielding when inductive coupling is considered. Also, it is shown based on the model and supported by simulations that the delay uncertainty decreases as inductance effects increase.
Chapter 4: Realizable Reduction of Interconnect Circuits

including Self and Mutual Inductances

Reduction of an extracted netlist is an important pre-processing step for techniques such as model order reduction in the design and analysis of VLSI circuits. This chapter describes a method for realizable reduction of extracted RLCK netlists by node elimination. The method is much faster than model order reduction techniques and hence is appropriate as a pre-processing step. The proposed method eliminates nodes with time constants below a user specified time constant. By giving the freedom to the user to select a critical point in the spectrum of nodal time constants, this method provides an option to make a tradeoff between accuracy and reduction. The proposed method preserves the DC characteristics and the first two moments at all nodes. It also recognizes and eliminates all the redundant inductances generated by the extraction tools. The proposed method naturally reduces to TICER [71] in the absence of any inductances.
4.1. Introduction

With increasing frequencies and faster signal transition times, on chip inductive effects are becoming increasingly important [1]-[6]. Consequently, many commercial and proprietary extraction tools, such as [57], generate $RLCK$ circuits for high performance designs. Due to the large amount of data typically generated by extraction tools, significant run time and memory issues affect the analysis tools. Therefore, in the past decade there has been a significant focus on model order reduction (MOR) methods, which attempt to model the extracted netlist by a smaller model with minimal loss in accuracy. Starting with AWE [60], methods such as [61] and [62] use moment matching - either explicitly or implicitly - and projection techniques to generate a low order approximation of the original circuit. More recently, PRIMA [63] modified these techniques to guarantee passivity of the reduced circuits.

Reducing an extracted netlist is an important step before the netlist is fed into tools such as AWE and PRIMA so that they run faster. In order to take advantage of the model order reduction techniques, it is important to have a realizable netlist reduction method, i.e. $RLCK$ in – $RLCK$ out feature. Realizability is important because this avoids the modification of mainstream analysis tools to handle reduced state-space or transfer function representations [65], since these tools are usually geared towards reading circuit netlists. Moreover, some analysis tools such as circuit checkers can only accept inputs in terms of $RLCK$ circuits. In addition to realizability, however, maintaining sparsity is also
important when reducing a circuit with a large number of ports. Even though the original circuit is large, it is very sparse since each node is only connected to a few nodes. It is important to maintain sparsity since model order reduction techniques perform better on sparse circuits.

Circuit reduction approaches based on Gaussian elimination include [66] and [68]. A different approach based on Gaussian elimination - called TICER - was presented in [71] for $RC$ circuits. By selectively removing the non-port nodes of the original circuit, a smaller, realizable, passive $RC$ circuit is produced. A method to reduce $RLC$ netlists with coupling-inductors was presented in [73], but it requires matrix inversion and long runtime. In this chapter, we extend the TICER approach to reduce general $RLC$ circuits including coupling-inductors using runtime in the order of the number of nodes in netlist. We also present a heuristic to control the sparsity of the reduced circuit. This is similar to the technique presented for $RC$ circuits in [66].

Most of the MOR techniques require moments calculation, which is computationally very expensive for large $RLCK$ netlists. Moments calculation requires inversion of large matrices, which may or may not be sparse because of coupling between nodes. This is a process with super-linear complexity. Although the reduced models still have to be produced after a large netlist is converted to a smaller one using the proposed realizable reduction technique, MOR techniques will be much faster on the smaller, reduced circuit. Computing moments of the reduced circuit will be much faster because it
requires inverting a much smaller system matrix, which has sparsity comparable to that of the original large $RLCK$ netlist. Hence, the main contribution of the work presented here is at the pre-processing level where MOR techniques and SPICE transient simulations are computationally very expensive in handling very large netlists. Once the netlist is pre-processed, there can be a significant reduction in run-time to produce reduced models from every source to every dependent sink or to simulate the circuit using SPICE.

The proposed method can also be easily embedded in extraction tools, most of which produce large parasitic netlists in the gigabytes size range due to a lack of good realizable reduction techniques for $RLCK$ netlists. These large parasitic netlists cause memory and runtime problems for many static timing analysis tools. The method proposed in this chapter solves the problem by reducing the size of netlists produced by extraction tools.

The presented reduction algorithm is much faster than model order reduction techniques and can be used as a pre-processing step for these techniques. The rest of the chapter is organized as follows. The underlying theory behind the proposed reduction method is discussed in section 4.2. In section 4.3, a high level algorithm for reducing $RLC$ circuits is presented. Experimental results are provided in section 4.4. Finally, section 4.5 concludes the chapter. The Appendix B describes the procedure to reduce $RLC$ circuits with coupling-inductors.
4.2. Theory

Consider a source free RLC circuit consisting of \( n \) nodes. The nodal voltages must satisfy the following equation in the \( s \)-domain:

\[
Y(s)V(s) = 0, \quad (4.1)
\]

where \( Y(s) \) is the \( n \times n \) admittance matrix. Consider the \( i^{\text{th}} \) node of the circuit and its \( k \) neighbors as shown in Fig.4.1(a). The \( i^{\text{th}} \) row of (4.1) is given by:

\[
Y_iV_i - y_iV_1 - y_2V_2 - ... - y_kV_k = 0 \quad \text{where} \quad Y_i = \sum_{j=1}^{k} y_j. \quad (4.2)
\]

![Fig.4.1 A general node in an RLC circuit. Admittances are added between node 1 and other neighbors of node \( i \) due to elimination of node \( i \).](image)

In order to eliminate \( V_i \) from the system (which is equivalent to eliminating the \( i^{\text{th}} \) node), we solve for \( V_i \) using (4.2):
Chapter 4: Realizable Reduction of Interconnect Circuits including Self and Mutual Inductances

\[ V_j = \left( \sum_{j=1}^{k} y_{j} V_j \right) / Y_i \]  
(4.3)

and substitute for \( V_i \) in the \( k \) equations where \( V_i \) occurs. Consider the first neighbor of \( i \). Its equation is now given by:

\[
(\hat{Y}_1 + y_{1} - y_{1}^2 / Y_i) V_1 - \left( \sum_{j=2}^{k} y_{1} y_{j} V_j \right) / Y_i - \sum_{r=1}^{k-1} y_{r} V_r = 0 , \quad \hat{Y}_i = \sum_{r=1}^{k-1} y_{r}
\]  
(4.4)

where \( \hat{Y}_i \) is the sum of all admittances from node 1 except to node \( i \) and \( k_1 \) is the number of nodes connected to node 1. The above equation can be simplified to

\[
\left( \hat{Y}_1 + \left( \sum_{j=2}^{k} y_{1} y_{j} \right) / Y_i \right) V_1 - \left( \sum_{j=2}^{k} y_{1} y_{j} V_j \right) / Y_i - \sum_{r=1}^{k-1} y_{r} V_r = 0 .
\]  
(4.5)

Note that this is equivalent to adding \( k - 1 \) new elements between node 1 and the \( k \) -1 former neighbors of node \( i \), (see Fig.4.1b). Specifically, for any two neighbors of node \( i \), say \( m \) and \( n \), the elimination of node \( i \) results in the addition of a new element between nodes \( m \) and \( n \), whose admittance is given by:

\[ y_{mn} = (y_{m} y_{n}) / Y_i . \]  
(4.6)

Thus, repeating this process for all the \( k \) neighbors of \( i \) will result in the addition of \( k(k-1)/2 \) new elements. Note that the elimination of node \( i \) may introduce a fill-in in the original \( Y \) matrix of (4.1). For instance, referring to (4.6), if the \( (m,n) \)th entry in \( Y \) was a zero, \( i.e., \) no element existed connecting \( m \) and \( n \), elimination of node \( i \) would produce a fill-in in the \( (m,n) \)th entry of \( Y \). In general, the formula for computing the fill-in, \( \phi_i \),
produced by eliminating node $i$ with $k$ neighbors is given by

$$\phi_i = k (k - 1)/2 - k - p.$$  

(4.7)

where $p$ is the number of elements connecting the neighbors of $i$ in the original system.

This type of nodal elimination preserves nodal voltages and equivalent branch admittance between nodes. Although the branch currents are not preserved explicitly, they are preserved implicitly because they only depend on nodal voltages and equivalent branch admittances, which are preserved. The new admittance given by (4.6) will be a polynomial in $s$. Without loss of generality for $RLC$ circuits (circuits with $K$ are discussed later), we assume that each admittance connecting a pair of nodes in the original system in Fig.4.1 consists of a resistor ($R$), inductor ($L$), and a capacitor ($C$) connected as shown in Fig.4.2.

![Fig.4.2 An admittance branch connected to node $i$.](image)

In most practical circuits, one or more of these elements will be zero. Note that this topology is general enough to handle any $RLC$ circuit including coupling capacitances. If no inductance is incident on the node, then (4.6) reduces to the TICER
case and we proceed as outlined in [71]. In that case (4.6) can be expressed by (4.8).

\[ y_{mn} = \left( g_m + sc_m \right) \left( g_n + sc_n \right) / \left( G_i + sC_i \right) \]  

(4.8)

where \( G_i = \sum_{j=1}^{k} g_j \) is the sum of all conductances to node \( i \), and \( C_i = \sum_{j=1}^{k} c_j \) is the sum of all capacitances to node \( i \). For pure \( LC \) case (4.6) can be expressed as

\[ y_{mn} = \left( \frac{b_n}{s} + sc_m \right) \left( \frac{b_n}{s} + sc_n \right) / \left( \frac{B_i}{s} + sC_i \right) \]  

(4.9)

where \( B_i = \sum_{j=1}^{k} b_j \) is the sum of all susceptances (reciprocal inductances) connected to node \( i \).

For every node in the circuit two time constants are defined: the \( RC \) time constant given by \( \tau_{RCi} = C_i / G_i \), and the \( LC \) time constant given by \( \tau_{LCi} = \sqrt{C_i / B_i} \). The nodal time constant at a node \( i \) is given by:

\[ \tau_i = \max(\tau_{RCi}, \tau_{LCi}) \]  

(4.10)

A node \( i \) is said to be a quick node if:

\[ \tau_i < \tau_{\text{min}} = 2\pi / \omega_{\text{max}}, \]  

(4.11)

where \( \tau_{\text{min}} \) is a user defined time constant below which a node is considered quick and depends on the maximum frequency of interest in the circuit, \( \omega_{\text{max}} \), as given above. The selection of \( \tau_{\text{min}} \) is circuit specific and is discussed in sections 3 and 4. According to (4.10) and (4.11), both time constants of a quick node must be less than \( \tau_{\text{min}} \). Note that \( \tau_{\text{min}} \) is proportional to \( 1/s_{\text{max}} \) as given by (4.11). Hence a quick node satisfies the
following approximations: \( sC_i < G_i \), \( G_i < B_i / s \), and \( sC_i < B_i / s \).

To eliminate a quick node with the above general RLC branch (Fig.4.2) two cases can be considered. In the first case, \( \tau_{RC_i} \) is much larger than \( \tau_{LC_i} \) and (4.8) can be used as in TICER [71]. With the quick node approximation (\( sC_i < G_i \)), (4.8) can be expanded into Taylor series upto first order:

\[
y_{mn} = \frac{g_m g_n}{G_i} + s \frac{c_m g_n + c_n g_m}{G_i} + \ldots .
\] (4.12)

Here the constant term in (12) gives the required conductance to be inserted between node \( m \) and \( n \) to eliminate node \( i \). The coefficient of \( s \) gives the capacitance value to be inserted. In the second case, \( \tau_{LC_i} \) is much larger than \( \tau_{RC_i} \) and (4.9) is used. Again with the quick node approximation (\( sC_i < B_i / s \)), (4.9) can be expanded into Taylor series:

\[
y_{mn} = \frac{1}{s} \frac{b_m b_n}{B_i} + s \frac{c_m b_n + c_n b_m}{B_i} + \ldots .
\] (4.13)

The coefficient of \( 1/s \) in (4.13) gives the required susceptance (reciprocal of inductance) to be inserted between nodes \( m \) and \( n \) to eliminate node \( i \). The coefficient of \( s \) gives the capacitance value to be inserted.

For the general case, when both \( R \) and \( L \) are present with \( C \) as in Fig.4.2, the rules for eliminating node \( i \) based on the equations (4.12) and (4.13) are shown in Fig.4.3. The values for the conductance and the susceptance come directly from the equations (12) and (13), respectively. But two expressions for capacitance are obtained from (12) and (4.13). If \( \tau_{RC_i} \) is larger than \( \tau_{LC_i} \) the expression for capacitance is taken from (4.12) and when \( \tau_{LC_i} \)
is larger than \( \tau_{RCi} \) the expression for capacitance is taken from (4.13). Therefore, all but one of the rules shown in Fig.4.3 for merging any two branches connected to a particular node \( i \) can be easily derived from (4.12) and (4.13). The exception is for the case when nodes \( m \) and \( n \) are connected to node \( i \) through capacitances. In that case the value of the capacitance to be inserted is \( c_m c_n / C_i \), which is the series combination of the capacitances.

Since only positive valued \( RLC \) elements are added during node elimination, the passivity of the reduced circuit is guaranteed by construction.

Fig.4.3 Rules for eliminating node \( i \)
In contrast to TICER, we do not consider the notion of slow nodes. This is because in practice the lowest frequency of interest is zero, i.e., the DC operation of the circuit is also required. In the following section, a high level algorithm implementing these ideas is presented. The appendix describes a method to reduce RLCK circuits, i.e. RLC netlists with coupling-inductors.

It should be noticed that the derivation of the above method of node elimination is based on two approximations, namely dominant $\tau_{RCi}$ and dominant $\tau_{LCi}$ approximations. Therefore, the correctness of the method is dependent on the validity of these two approximations. If for any node the two time constants ($\tau_{RCi}$ and $\tau_{LCi}$) are far from each other the proposed method will work very effectively. If the two time constants are comparable (rarely happens in practice) then the reduction will introduce larger error. In such situation it is suggested not to eliminate that node if very low error is required. Therefore, to eliminate a node from the net list with less error two criteria have to be considered. First the node has to be a quick node, and second the two time constants ($\tau_{RCi}$ and $\tau_{LCi}$) should not be comparable. Tuning the threshold for these two conditions produces a tradeoff between accuracy and reduction.
4.3. Reduction Algorithm

The high-level reduction algorithm is shown in Fig.4.4. All the nodes in the original circuit are stored in a priority queue with the node with the smallest nodal time constant at the head of the queue. In addition to checking for the time constant of the node, we also check if the fill-in due to this node is less than some user specified threshold $\phi_{\text{max}}$. If unspecified this threshold defaults to zero. This heuristic is added to ensure that the admittance matrix of the reduced circuit remains sparse. Of course, this heuristic may cause the algorithm to get stuck in a local optimum where even though a node’s time constant may be less than $\tau_{\text{min}}$, it may fail the fill-in check. However, for most interconnect circuits, such as those with a tree like topology, this algorithm will produce reasonably sparse reduced circuits. On the other hand, for very dense topologies where each node has several neighbors, the efficiency of reduction will be less with because of the fill-in criteria and the algorithm will perform poorly. However, this same problem also occurs in TICER for $RC$ circuits. The main contribution here is the extension of TICER to circuits with $L$ and $K$ elements and controlling the density of system matrix through the fill-in criteria. While not explicitly shown in Fig.4.4, certain non-port nodes may also be marked as required by the user in which case these nodes cannot be eliminated. A check for this can be easily added to the algorithm.
One natural question arises regarding the choice of $\tau_{\text{min}}$. Higher the value of $\tau_{\text{min}}$, higher frequency components get eliminated and higher the loss of accuracy. While signal transition times and operating frequencies do play a part in the choice of $\tau_{\text{min}}$, a histogram showing the distribution of the time constants can be very helpful. As we show in the next section, a large number of nodes typically have very small time constants. By choosing $\tau_{\text{min}}$ appropriately, these nodes can be eliminated with almost no loss in accuracy. A histogram helps in placing the time constants of all the nodes in the circuit in perspective as described in the next section.

**REDUCE_NETLIST** ($\tau_{\text{min}}, \phi_{\text{max}}$)

1. Place all non-port nodes of the circuit in a priority queue sorted by local nodal time-constants.
2. $i = \text{head of the priority queue}$
3. while (queue is not empty AND $\tau_i < \tau_{\text{min}}$ AND $\phi_i < \phi_{\text{max}}$)
4. set $S = \{\text{neighbors of } i\}$
5. if ($1/B_i == 0$)
6. eliminate $i$ according to the TICER quick-node rules in [71]
7. else
8. eliminate $i$ according to rules in Fig.4.3
9. end if
10. update time-constants of nodes in set $S$ (neighbors of $i$)
11. $i = \text{head of the priority queue}$
12. end while

Fig.4.4 Circuit reduction algorithm
The main essence of this proposed method is speed. Making the method mathematically more robust and having a more robust technique to determine $\tau_{\text{min}}$ will only increase the complexity of calculation without significant improvement in accuracy. This complexity may destroy the main essence of the proposed technique. That is why the technique is devised based on heuristic approach rather than utilizing intense mathematical calculation. Simple approach like plotting a histogram is an easy way to determine a good $\tau_{\text{min}}$. 
4.4. Results

We implemented the reduction algorithm in C++. Specifically, $p$ was assumed to be zero in (4.7). We also required $\phi_{\text{max}} = 0$, which guarantees no refills by the reduction algorithm and maintains the sparsity of the $Y$ matrix. Therefore, only nodes with a degree less than or equal to three were candidates for elimination. By applying the methods on some small industrial circuits (Table 4.1 and Fig.4.6) with less than 500 hundred nodes an average 50% reduction of circuit elements and nodes is obtained with less than 1% error in rise time and delay calculation.

![Sample waveforms from (a) Small industrial circuit](image-url)

Fig.4.5 Sample waveforms from (a) Small industrial circuit
Fig. 4.6 Sample waveforms from a Medium industrial circuit

Table 4.1. Small and medium size industrial circuits.

<table>
<thead>
<tr>
<th></th>
<th>Small industrial circuit (less than 100 nodes)</th>
<th>Medium industrial circuit (several hundred nodes)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Original</td>
<td>Reduced circuit for different $\tau_{\text{min}}$ (ps)</td>
</tr>
<tr>
<td>$\tau_{\text{min}}$ (ps)</td>
<td>-</td>
<td>0.002 20 200</td>
</tr>
<tr>
<td>Nodes</td>
<td>81 55 43 29</td>
<td>227 158 147 127</td>
</tr>
<tr>
<td>Total Elements</td>
<td>152 105 79 54</td>
<td>526 290 271 241</td>
</tr>
<tr>
<td>% Reduction of nodes</td>
<td>-</td>
<td>32 47 64</td>
</tr>
<tr>
<td>% Reduction of elements</td>
<td>-</td>
<td>31 48 64.5</td>
</tr>
<tr>
<td>% Error in Rise Time</td>
<td>-</td>
<td>0.02 0.8 0.7</td>
</tr>
<tr>
<td>% Error in Delay</td>
<td>-</td>
<td>0.36 0.36 11</td>
</tr>
</tbody>
</table>
The drivers and loads chosen here were based on typical design guidelines for high performance microprocessor circuits. The range of driver impedances was comparable to the impedance range of the interconnect netlist. If the allowable margin of error is around 3% an average reduction of 55% can be achieved by selecting a higher $\tau_{\text{min}}$. Higher error tolerance (around 5% and higher) will give even higher reduction in the range of 55% to 70%.

For symmetric and uniformly distributed $RLC$ networks this method will give very high reduction. For a balanced and uniform H-tree network a reduction of about 90% is obtained with almost 0% error (Table 4.2 and Fig.4.7). With this amount of reduction a twenty-fold decrease in simulation time is obtained. Such a high reduction of the simulation time is due to the symmetric and uniform nature of the original and resultant reduced circuits.

### Table 4.2. Balanced and uniform H-tree networks

<table>
<thead>
<tr>
<th>$\tau_{\text{min}}$ (ns)</th>
<th>Original</th>
<th>Reduced circuit for different $\tau_{\text{min}}$ (ns)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0.1 0.5 1</td>
<td></td>
</tr>
<tr>
<td>Nodes</td>
<td>2502</td>
<td>666 416 128</td>
<td></td>
</tr>
<tr>
<td>Total Elements (R: 1250, L: 1250, C: 1250)</td>
<td>3750</td>
<td>997 617 190</td>
<td></td>
</tr>
<tr>
<td>% Reduction of nodes</td>
<td>-</td>
<td>73.4 83.37 94.9</td>
<td></td>
</tr>
<tr>
<td>% Reduction of elements</td>
<td>-</td>
<td>73.4 83.54 94.9</td>
<td></td>
</tr>
<tr>
<td>% Error in Rise Time</td>
<td>-</td>
<td>0.00 0.01 0.03</td>
<td></td>
</tr>
<tr>
<td>% Error in Delay</td>
<td>-</td>
<td>0.00 0.00 0.00</td>
<td></td>
</tr>
</tbody>
</table>
Chapter 4: Realizable Reduction of Interconnect Circuits including Self and Mutual Inductances

The above small and medium sized circuits do not give clear idea of speed up (reduction of actual simulation time) due to nodes and elements reduction. With these objectives in mind the method is applied to an extracted clock distribution network from a commercial high-performance microprocessor. The extracted circuit contained over 678,608 elements and more than 10,000 sinks. A histogram of the distribution of the nodal time constants of this circuit up to a maximum of 100ps is shown in Fig.4.8.

Based on this histogram, we made three choices of \( \tau_{\text{min}} \) for circuit reduction: \( \tau_{\text{min}}=15 \) ps, \( \tau_{\text{min}}=25 \) ps, and \( \tau_{\text{min}}=35 \)ps. The results of running RICE (v5) [59] on the original as well as the three reduced circuits are shown in Table 4.3 for an input rise time.
of 50ps. A fourth order approximation was computed at every sink. Clearly $\tau_{\text{min}} = 15$ ps offers the best choice resulting in over three times decrease in analysis time with almost no loss in accuracy. These reductions in run-time are expected to be much higher when non-linear elements are combined with the interconnects. Note that the reduced RLC circuit can be readily inserted in any simulator such as SPICE or AS/X. As expected, choosing larger values of $\tau_{\text{min}}$ resulted in a loss of accuracy. Besides improving the analysis time, the reduction algorithm also reduced the storage requirements by one-third.

![Distribution of Time Constants](image)

Fig.4.8 Distribution of time-constants for different nodes of a clock distribution network
Table 4.3. Reduced commercial circuit statistics

<table>
<thead>
<tr>
<th>tau_{min} (ps)</th>
<th>Original</th>
<th>Reduced circuit for different tau_{min} (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>Nodes</td>
<td>380K</td>
<td>148K</td>
</tr>
<tr>
<td>Total Elements</td>
<td>679K</td>
<td>285K</td>
</tr>
<tr>
<td>(R: 368K, L: 72K, C: 239K)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>% Reduction of nodes</td>
<td>-</td>
<td>60.8</td>
</tr>
<tr>
<td>% Reduction of elements</td>
<td>-</td>
<td>57.9</td>
</tr>
<tr>
<td>% Error in Rise Time</td>
<td>-</td>
<td>0.05</td>
</tr>
<tr>
<td>% Error in Delay</td>
<td>-</td>
<td>0.25</td>
</tr>
<tr>
<td>Speedup</td>
<td>-</td>
<td>3.23</td>
</tr>
</tbody>
</table>

Fig.4.9 % Error vs. reduction
The average reduction at different levels of error in delay and rise time calculation is shown in Fig.4.9 from the reduction statistics of all the circuits presented above. It is observed that if the error is limited to 1%, an average reduction of 60% is obtained. If the error is allowed to go up to 3%, an average reduction of 66% is obtained. At 5% error, average 67% reduction can be achieved. It is observed from Fig.4.9 that beyond 67% reduction point, for a smaller gain in reduction a very high error is introduced. This is because at these amounts of reduction many critical circuit nodes and elements are thrown out of the netlist. Consequently the circuit behavior changes sufficiently and very high error in performance evaluation occurs.

The RLCK node elimination scheme (see Appendix) was applied to a 16-bit coupled bus with 18,000 elements (3200 \( R \), 3200 \( L \), 3200 \( C \), 8400 \( K \)) including coupling-inductors and 9617 nodes. The circuit was reduced down by 94% with the new circuit having 189\( R \), 205\( C \), 189\( L \), and 916\( K \). The results show that the method reduces the number of coupling-inductors by as much as 89%. A sample output for a middle bit is shown in Figure 9. The output signal for the reduced circuit is almost identical to the signal in original circuit with 18,000 elements. Error in rise-time and delay was almost 0%. The results for other nodes are also very accurate.

The results for cross-talk prediction are also very accurate using the reduced circuit. Fig.4.11 shows the noise on a victim bit-line of the 16-bit coupled bus because of an aggressor bit-line switching. The noise curve given by the reduced circuit is almost
identical to the noise curve given by the original circuit. The results are very similar at other nodes also. These accurate results on 94% reduced $RLCK$ bus show that the proposed method is highly applicable to circuits with coupling-inductors. Not only a large 89% reduction in the number of coupling inductors is achieved, but the reduced circuit also gives signals that are almost identical to those produced by the large original netlist.

Fig.4.10 Sample waveform from 16-bit coupled $RLC$ bus with coupling-inductors
4.4: Results

![Graph showing noise on a victim bit-line of the 16-bit coupled bus.]

Original and 94% reduced \( RLCK \) circuits give almost identical results.

Fig. 4.11 Noise on a victim bit-line of the 16-bit coupled bus.
4.5. Conclusion

This chapter presented a realizable reduction method of $RLC$ circuits (with coupling-inductors) by nodal elimination. This method is useful in analyzing and verifying large $RLC$ networks. If model order reduction is not realizable it produces reduced mathematical model of transfer function or reduced state equations. Hence all downstream circuit simulation and associated tests have to be modified to handle these reduced mathematical representations of the circuits. Since the proposed realizable reduction method is an $RLCK$-in to $RLCK$-out, all standard simulators can handle the reduced circuits without any modification. Reduced netlist also guarantees faster simulation, lower memory and storage requirements. It is shown that for an average of 40% to 50% reduction of nodes and elements, the error in waveform shape calculation is less than 1%. If 3% error is allowed, a reduction of about 60% to 70% is obtained. Higher allowance of error results in an even higher reduction. Therefore, the user has the freedom to make the trade-off between accuracy and speed. Circuits with coupling-inductors are also reducible with the presented algorithm (see Appendix) and the results are very accurate for aggressor as well as victim nets.
Chapter 5: Circuit and Signal Integrity Challenges in Systems-On-a-Chip

Advances in deep sub-micron technologies together with the ability to provide on-chip interfaces between characteristically conflicting blocks for multiple functionalities, is leading the semiconductor world to an era of System-on-a-Chip (SoC). Due to the increasing popularity of wireless and handheld applications, gradually Systems-on-a-Chip is becoming a reality. This chapter surveys the challenging issues that the designers have to solve to design a complex system on a single IC. The focus of this chapter is mainly on the physical and circuit level issues like isolation, substrate noise, interconnect coupling, related complexities, and possible solutions.
5.1 Introduction

Due to the increasing popularity of multimedia and communications applications like speech recognition, video compression, adaptive cellular phones, and the explosive growth of various other handheld devices, aggressive design goals such as lower power, higher-speed, and lower-cost are inevitable. In order to achieve these goals, most portable systems must have “System-on-a-Chip” (SoC) capabilities, requiring the integration on a single chip of digital processors, memories, interconnects, buses, analog front ends, RF and microwave circuits, DSPs, MEMS, optical I/Os, embedded passive elements ($R$, $L$, $C$), and various interfaces (see Fig.5.1 [95],[7]. Personal device assistant (PDA), digital cameras, smart cars, and digital theaters are some candidates for the applications of SoC technologies [96].

There are many historical developments of the semiconductor technology that have occurred during the last few decades, which have built the path for SoC (see Fig.5.1). In early 1960s, when the first generation of Integrated Circuits (Operational amplifiers and basic gates) came out, probably no one could imagine that the semiconductor industry would reach the point where it is now. Between Moore’s law (1965) and the year 2000 the number of transistors per chip increased from a few dozens to more than 100 million, and the cost per transistor came down to millionth of a dollar. Future deep sub-micron technologies will enable the implementation of exceedingly complex ICs with billion transistors and enormous computing power. ICs would no
longer be stand-alone components dedicated to a particular function, but huge chips with all aspects of a system. Designers are attracted to this new concept of building systems similar to using integrated circuits on a printed circuit board (PCB), because of the ability to provide RF and analog interfaces with the digital cores. In recent years libraries of pre-designed, pre-verified building blocks (embedded cores or virtual components) were developed to import new technologies to a new system and differentiate the corresponding product by leveraging intellectual property advantages [97].

Fig.5.1 Development of VLSI systems from 1960 to 2000. With the turn of the century, SoC is becoming a reality.
The challenges and issues that have to be addressed for the successful implementation of SoC are as follows: (a) Integration, testing and interoperability problems; (b) EDA tools for analysis, testing and verification; (c) intellectual property issues, and business and legal challenges; and (d) circuits and signal integrity (noise) issues. In section 5.2 the first three groups of issues are briefly discussed. The last and the most important issues related circuit and signal integrity are addressed in details in section 5.3. Finally, section 5.4 concludes this chapter.
5.2 Issues and Challenges of System-on-a-Chip

5.2.1 Integration and Interoperability

There are strong similarities between the traditional System-on-Board (SoB) and SoC [98]. The functionality of each of the cores of a SoC can be directly translated to an actual IC component on the traditional System-on-Board. However, this is where the similarities end. In PCB-based design, the system integrator is only responsible for designing and manufacturing a system out of tested and fault-free ICs by providing interconnections between components (individual ICs). But in case of SoC, the core provider delivers virtual components – a description of the core design. It is not possible for the provider to test his core, simply because it is not yet manufactured. In most cases the virtual components come in the form of hard or encrypted cores, where the system integrator can only treat the core as a black box. Virtual components can also be soft or firm, with different levels of description and abstraction [97]. The integration of cores into SoC is largely a manual and error prone process because it requires designers to fully understand the functionality, interfaces and electrical characteristics of complex cores. Any interface or functional problem in traditional SoB can be rectified with glue logic or a board rework, which is not possible for SoC [98]. Various interface and timing issue can cause systems to fail even though individual cores are correct. That is why the interoperability issue in actual system environments is one of the major problems in a
core-based system. Increasing the integration of analog and digital circuitry causes a struggle to maintain analog signal integrity. To achieve full interoperability, proper routing, and interconnections network among cores should be provided, which may cause unforeseen effects such as substrate noise, coupling capacitances and inductances among interconnect lines, and coupling through power and ground rails.

All of the recent studies including semiconductor technology Roadmaps [7], indicate that in a SoC environment, there will be heterogeneous technology mix; signal and frequency mix; and also design and architectural mix. By putting all the discrete components on the same chip, the physical distances are removed, which ensures faster response, and robust and reliable operation. However, integrating all these separate components is not an easy task. Traditionally, analog circuitry has been implemented with technology that is at least one or two generations behind the current, state-of-the-art digital process. With the explosion of wireless communications devices, such luxuries can no longer be afforded. As a result, the analog portions of the SoC are now being designed with the same short channel devices as their digital counterparts. Under these conditions, analog design will face greater hot electron degradation, which leads to lower output gain, and greater mismatch in differential amplifiers and current mirrors over time. In addition, the continuous reduction of the power supply to reduce short channel effect, also limits the amount of amplification required for analog designs. Therefore, more amplification stages have to be added, increasing area and power consumption. Many
state-of-the-art technologies now have dual-mode power supplies with lower voltage supply for the digital portion and higher voltage supply for the analog portion. With the combination of short channel length and high power-supply voltage, analog circuit aging will be exacerbated. Furthermore, the large amount of digital switching power caused by the digital section will further impact the analog circuits.
5.2.2 EDA Tools Requirements for SoC Analysis, Testing and Verification

Current formal verification as well as software simulation techniques does not have the necessary capacity or speed to handle large systems in short time. Hardware-Software integration is another problem, which directly affects manufacturing and marketing time because it is usually done in a later phase when the hardware part is more stable. Most of the CAD tools are traditionally stand-alone tools focused on low-level design issues such as modeling, synthesis, simulation, timing, and layout. These tools take proprietary data formats, which are not compatible with various data formats of virtual components, and are hence not suitable for systems using cores. Many vendors in the EDA tools business declared some tools for modeling, simulation and testing of cores; but there is no industry-wide standard. This lack of industry-wide established standard and the lack of efficient synthesis tools makes it difficult for virtual components from different providers to be integrated on the same substrate. For these reasons, standardization of these diverse data formats is a major concern. Verification, test development, and test application for SoCs are complex tasks, for which tool assistance is needed [98], [103]. EDA tools must be capable of handling libraries of pre-verified and tested standard cores from different sources. Effective automation tools have to be developed for test and validation.
5.2.3 Intellectual Property Issues, Business and Legal Challenges

In the semiconductor industry, design productivity is a key requirement for any successful implementation of a new system. Whenever time to market is a key factor, design reuse and virtual core exchange, and related intellectual property protection problems should be taken care of properly for commercial implementation of SoCs. To protect IP, encryption is one of the best methods; but for integration in SoC, unprotected forms of cores are needed, which calls for establishing proper exchange modes between core provider and core user to protect financial benefits and copyright of the respective parties. Effective automation tools have to be developed for test and validation.

All these issues are territorial problems and can be solved by proper cooperation among diverse groups. Virtual Socket Interface Alliance (VSIA), a forum of all major players in semiconductor industry and research, already started laying the groundwork for open standards. Many EDA vendors are offering newer tools for test and validation. Different companies, research groups and alliances already created enough optimism among people in this field. But the central and internal issue that must be solved for successful implementation of SoC is the circuit and signal integrity issues, which are discussed in the next section.
5.3 Circuit and Signal Integrity (Noise) Issues

This section addresses issues regarding substrate coupling, noise through power and ground rails, interconnect coupling and possible solutions. Subsection 5.3.1 covers substrate noise, and subsection 5.3.2 briefly discusses coupling through power and ground rails. Subsection 5.3.3 discusses interconnects issues.

5.3.1 Substrate Noise

The parasitic interconnect capacitance of the $V_{ss}$ rail that biases the bulk can be a significant pathway for injecting substrate noise [99]. Digital switching causes noise coupling through common substrate, which is both difficult to measure and difficult to control. Substrate noise-conduction modes in mixed signal ICs can be classified as follows: (a) resistive coupling, (b) capacitive coupling, (c) impact ionization and (d) body effect (see Fig.5.2). In case of both digital and analog cores, if the bulk is biased with a switching ground bus, switching transients will couple the cores resistively through the p+ bulk contacts. The parallel summation of bulk contacts and epitaxy resistances provides a very low impedance path (nearly short) to the p+ buried layer. The second and most serious source of substrate noise is capacitive coupling through the substrate p-n junctions. The MOSFET source and drain form a p-n junction with bulk. Each n-well on p+ bulk also introduces fairly large p-n junction – this cause a capacitance between the
5.3.1: Substrate noise

$V_{DD}$ rails biasing the n-well and the $V_{SS}$ rails biasing the bulk. The junction capacitance for one transistor is fairly small, however many transistor are connected to the same $V_{SS}$ rail. Depending on the chip size and technology process, the total parasitic junction capacitance can be significantly large. Another source of substrate noise in digital cores is impact ionization current, generated at the pinch-off point of the NMOS transistors. Impact ionization causes a hole current in the bulk. If the analog ground rail does not bias the bulk, then body effect will couple substrate noise into analog circuit. In that case, a negative bulk transient will increase the depletion region between the source and bulk. This depletes the channel of charge carriers and increase $V_{th}$. The total effect is a sporadic decrease in the $I_{DS}$ current.

Fig. 5.2 Mechanisms of substrate noise propagation in mixed signal ICs
Chip designers apply various methods to minimize the effects of substrate noise and coupling through power and ground rails. One way to minimize the parasitic junction capacitance is to tie up the bulk and the source together. To eliminate the body effect the analog bulk can be tied up to $V_{SS}$ rail. Increasing the analog $V_{SS}$ capacitance to bulk can be a good alternative. The higher capacitance will lower the bulk-to-source voltage transient, thereby reducing the body effect. Also, since the n-well capacitance is much higher than the bulk-to-source capacitance, adding capacitance from the analog $V_{SS}$ to the bulk will help balance the coupling into each rail. This “balanced capacitance” will reduce the effective noise seen across the analog power rails [99]. In the CMOS epitaxial process, a highly doped substrate is used to increase latch-up immunity. But a highly doped substrate provides a very efficient conduction path for substrate noise. P+ buried layer collects and distributes noise throughout the integrated circuit. Since the majority of the substrate noise propagates through this path, separating the sensitive and perturbing nodes of the circuit provides very little improvement in noise immunity. Isolation techniques like Silicon On Insulator (SOI) and junction isolation show bright promise for future generations of mixed-signal design. Recent trends in semiconductor technology indicate that the SOI technology is a potential solution for System on a chip.

An SOI device is composed of a thin layer of Si film (ranging from 10 nm to 1000 nm depending on its application) that is on top of a thick electrically insulating silicon dioxide layer called buried oxide (BOX) (typically, 80 nm to 1 µm thick). Many of the
challenges facing bulk Si CMOS transistors as discussed above will be either relaxed or
eliminated by using SOI technologies. SOI devices with their unique structure offer very
palpable advantages, such as (1) lower junction capacitance which means faster circuits,
(2) eliminating substrate coupling up to 10 GHz [100], (3) steeper sub-threshold voltage
slope, higher ON current, and lower OFF current due to the dynamic threshold
characteristics, (4) reducing short channel effects, (5) absence of body effect and latch up,
(6) lower soft-error rate which is essential for DRAMs, and (7) simpler isolation
techniques that lead to higher packing density [101]. Due to the recent developments in
low cost, large size SOI wafers (SIMOX, UNIBOND by LETI, BESOI by IBM and
Toshiba, and the recent 300mm Eltran SOI wafers made by Canon [86]), SOI is
becoming a leading candidate for portable low power, low-voltage, and high-frequency
mixed signal devices. IBM also has proposed using BiCMOS and SiGe HBT to give SOI
technologies higher flexibility in building high performance SoC.

There are two kinds of SOI MOSFET devices as shown in Fig.5.3. The first one is the
Partially Depleted (PD)-SOI device, which is very similar to bulk-silicon in terms of
fabrication and current characteristics. The other type is the Fully Depleted (FD)-SOI
device, which could be easily used with existing bulk-Si circuit design techniques. Other
SOI technologies such as dynamic-threshold (DT) and double-gate (DG) technologies
give SOI additional flexibility in future ULSI applications [87]. In the case of PD-SOI
devices, the depletion charge controlled by the gates does not fully extend through the
silicon layer. If body contacts are not properly placed, floating body effect will occur, which causes kink effect [88], anomalous sub-threshold currents [9] as well as early device breakdown. Kink effect lowers the threshold voltage, which leads to higher output current but lower gain in analog circuits, which is highly undesirable in mixed signal devices [89]. Over the years, a number of methods have been proposed to either eliminate or minimize this effect such as implanting $Ar$ to reduce minority carrier lifetime [87], implanting $Ge$ into the source or drain regions to reduce the energy band gap [89], i.e. reduce minority carrier lifetime, and using different body tie methods [90] which results in larger area. Despite all these disadvantages, PD-SOI is the best SOI technology for device scaling below 0.18 μm due to better source and drain resistance as well as stable and multiple threshold voltages, which can balance performance against noise and power. IBM, Motorola and AMD are currently using PD-SOI devices for their latest microprocessor designs.

On the other hand, the depletion charge in FD-SOI device is constant and covers the whole Si layer. Although it has good short channel characteristics and soft floating body effects compared to PD-SOI devices, the output gain of an FD-SOI device is significantly lower for analog amplifiers. Also, the sub-threshold latch, higher flicker noise and large threshold variation due to the non-uniformity of the thin Si film remain unsolved [91]. Some researchers are using dual body SOI structures for mixed signal circuits with PD-SOI devices for analog applications and FD-SOI devices for digital application [92].
However, this structure has many challenges due to fabrication, circuit design complexity and the inherent problems facing FD-SOI devices scaling below 0.18 µm. Thus, using PD-SOI devices below 0.18 µm is preferable [93].

5.3.1: Substrate noise

There are still some obstacles facing PD-SOI technologies in the circuit level beside the floating body problem:

(i) **Self-heating:** Due to the presence of buried oxide in SOI devices, the thermal conduction to the substrate will be reduced. This will increase the device temperature, with corresponding reduction in device performance and reliability.
(ii) Pass-Gate leakage current: Pass-gate leakage current usually occurs in NMOS when the gate electrode is off and both source and drain electrodes are high for few milliseconds, the body will accumulate holes up to $V_{DD}$ through diode leakage. If the source is pulled low, a transient forward bias appears between the source-body diode, which leads to a parasitic current. This current can cause a number of failures in DRAM circuits and wide NOR gates [94]. This current can be minimized by using fabrication techniques such as proper source-body diode doping or by using circuit methods such as increasing the size of write drivers, or limiting the number of cells in a bit line [93].

(iii) Reduction noise margin: Because of the floating body effect of PD-SOI devices, there exists a forward bias between the body and the source, which leads to the reduction of threshold voltage. This will make SOI devices faster but more susceptible to noise.

(iv) Electrostatic discharge: When devices are insulated from the substrate by silicon oxide, special electrostatic protective circuits need to be added since silicon dioxide is two orders of magnitude worse than Si in terms of thermal and electric conduction. Although SOI still has many challenges and obstacles, it is a viable solution for building low-power, high-speed system-on-a-chip devices because of its unique structure, which eliminates junction capacitances and substrate crosstalk.
5.3.2 Coupling Through Power and Ground Rail

Noise through power and ground rails is another source disturbance that has to be taken care of by the SoC designers. Introducing decoupling capacitance close to chips on PCB-based system is a well-established method to reduce $LdI/dt$ noise. Similarly, in the case of SoC, on-chip decoupling capacitance can be provided to reduce the effect of the inductance in the power supply path [27]. With continuous scaling of the minimum feature size, increasing die size, and dramatically increasing number of transistors on a chip in core-based systems, the inductance of the power and ground rails is increasing. This implies that on-chip decoupling capacitance will be required in the future unless new packaging techniques can dramatically reduce the power supply inductance.
5.3.3 Interconnect Coupling

The increasing global interconnect lengths is already a major concern in designing integrated circuits. In the new era of SoC, this issue will present an even greater challenge, since the designer now have to provide complex interconnects between diversely varying cores as well as interconnects within each core. Long global interconnects will be dominant in future SoCs due to the rapid increase of the number of components or cores. In a typical SoC, several bus structures are required to ensure interoperability of the diverse cores as shown in Fig.5.1. Blocks like ALUs, multipliers, shifters, instruction decode units, and program counters inside a CPU communicate through numerous busses. At the system level the cores communicate using a hierarchy of busses, having different bandwidths, speeds, power and other characteristics. The use of deep sub-micron technologies and the increase of clock frequencies in SoC increase capacitive and inductive coupling between switching nets, which leads to severe affects on signal integrity (see Fig.5.4). When coupling capacitance becomes a first order parameter between two bus lines, two basic signal anomalies can take place. If one line is switching and the other line is steady the energy transfer through the coupling capacitance results in glitch on the quiet line. The second anomaly, when the two lines are switched in opposite direction, the result is an increase in transition time, leading to higher delay. When inductance is combined with other elements of the circuit model, the voltage relationship generally results in a higher order differential equation. In addition to
glitches and delays, the solution may result in underdamped oscillations superimposed on top of a glitch or delay [3]-[5].

Fig. 5.4 Effect of interconnect coupling

Fig. 5.5 Circuit model for two adjacent interconnects
To avoid degrading the interconnect resistance, the vertical dimensions of metals has scaled slowly as compared to the horizontal dimension, leading to extremely high height/width aspect ratios. At the same time with technology scaling, motivated by speedup requirements, the line to ground capacitance of individual devices and local interconnect is decreasing [20], leading to higher current injection due to coupling. Fig.5.5 illustrates all the factors, which influence the interaction of two adjacent interconnects $I_1$ and $I_2$. In sub-micron technologies, driver resistances $R_1$ and $R_2$, line-to-ground capacitances $C_1$ and $C_2$, and inductances $L_1$ and $L_2$ for each interconnect and the driver resistance $R_{ON}$ together with the load capacitance will dominate the circuit behavior. However, in deep sub-micron technologies cross talk due to the coupling capacitance $C_C$ and mutual inductance $M_{12}$ between lines will become equally important. The degree of cross-talk depends on several factors such as the driver strength $R_{ON}$, line length and width, line spacing, clock speed, skew, driver balance, load to load balance, and impedance matching, etc. Modern trends are leading to increasing length, diminishing spacing, and increasing height and higher metal aspect ratios of global interconnects within the cores and at the system level [3]. Consequently, coupling noise increased dramatically and delays due to coupling capacitances and mutual inductances have not kept pace with the speedups in transistors due to technology scaling [5].

Several design technique including physical design and automation tools are being developed to help minimize the signal integrity problem. Inserting repeaters to divide the
interconnect lines into shorter sections is a well-accepted technique to minimize the effects of increasing interconnects parasitic (R, L, C) [4]. Providing shielding between interconnects, increasing line spacing at the expense of die size, and introducing buffers to eliminate noise effects are some techniques adopted in the digital domain. These techniques can be extended in the broad area of SoC. Traditionally, in the digital domain, device defects use abstract models such as stuck-at-faults. However, with the emergence of previously negligible electromagnetic induction effects that introduce analog behavior, earlier techniques are not that effective now. Even if cross-talk noise is minimized during design, process variations and defects during manufacturing may introduce new factors such as bridging resistance and floating nets, which can cause excessive cross-coupling capacitance and inductance between interconnects, resulting in increased noise effects.
5.4 Conclusion

Due to the continuous progress in deep sub-micron technologies it seems very promising to implement exceedingly complex ICs with billion transistors and enormous computing power, which would no longer be stand-alone components dedicated to a particular function, but huge chips with all aspects of a system. However, realization of whole system on a single chip will impose numerous design and implementation challenges. A review of the issues and challenges related to SoC is presented in this chapter. Among the various issues, this chapter emphasizes circuit and signal integrity issues, since they will become more profound in the future technologies. Signal integrity and noise will limit the minimum magnitude of a signal that can be amplified by an analog core. It will also limit the upper bound of the effective gain of an amplifier. In digital parts, noise can change logic information temporarily or permanently. It can also cause problems like changing time delay, increasing power dissipation, and bootstrapping. Various performance bottlenecks and possible solutions are discussed. Existing methods can be extended or new techniques must be developed to deal with new set of performance matrices that will arise in the SoC domain. In industry design productivity, cost and time to market are key requirements for any successful implementation of a new system. Therefore, design reuse and virtual core exchange, and related intellectual property protection problems should be taken care of properly, which calls for establishing proper exchange modes between virtual or soft core provider and core user to protect financial benefits and copyright of
the respective parties. Effective automation tools have to be developed for analysis, test and validation. Industry-wide standard can be established through forum like Virtual Socket Interface Alliance (VSIA). Extensive collaboration among various research, industrial and vendor organizations and individuals can lay the groundwork for open standards. Despite all these challenges, SoC promises to revolutionize the design of electronic products. There is a significant potential for SoC as a vehicle to incorporate all aspects of integrated circuits in one chip and developing new electronic products to meet the growing needs of small handy systems.
Chapter 6 : Analysis of Coupling Noise in Dynamic Circuits

The usage of noise sensitive dynamic circuits has become commonplace due to speed and area requirements, making the noise issue even more prominent. This paper focuses on the trends of coupling and its effects on dynamic circuits. The paper presents closed form analytical solutions for noise as well as noise tolerance metrics for dynamic circuits. These solutions are within 5% of dynamic simulations. It is shown that not all scaling trends are negative for noise, and that the scaling down of supply voltage and increasing frequency help improve certain aspects of the noise immunity of dynamic circuit. Most of the work treated the noise immunity and the noise content separately. This paper introduces an analysis of noise scalability by looking at the noise immunity and the noise content simultaneously.
6.1. Introduction

With the continued scaling in modern deep submicron CMOS processes, noise has become an equally important metric to area, timing and power dissipation [27]-[36],[50],[51]. Performance requirements are driving designs in the direction of using noise-sensitive dynamic circuits, making the analysis of noise effects more important. Dynamic logic is gaining popularity for its attractive features of reduced transistor count with a reduced capacitive load resulting in lower area and increased speed for CMOS circuits [27]. In static circuits momentary deviation of logic levels can be restored automatically, since at steady state the nodes are always connected either to ground or $V_{dd}$. However, this restoration is not possible in dynamic circuits due to the possibility of floating nodes. Fig.6.1 illustrates the susceptibility of dynamic logic by a simple example of two inverters. Because of the dramatic reduction in the supply and threshold voltages with the continuous scaling of CMOS technologies, the noise margins have been significantly decreased. In static logic the $N$ and the $P$ blocks can be balanced to obtain the highest possible noise margins. But in the case for dynamic logic, the noise margins can be as low as $V_{tn}$. Lower threshold voltages also result in increased leakage noise.
Among the various sources of noise in current deep submicron CMOS technologies the noise due to capacitive and inductive coupling has become dominant [108]-[110]. Coupling noise imposes two serious side effects on digital integrated circuits. Coupling can cause the effective line capacitance and inductance to increase or decrease in the presence of simultaneously switching coupled lines, increasing or decreasing the signal delay. Second, it can cause functional failures by charging or discharging the capacitor responsible for holding the logic level at a dynamic node. To analyze the effects of coupling it is not the absolute value of the coupling capacitance that has to be considered.
The two factors, that affect circuit performance, are (i) the ratio between the coupling capacitance to the total capacitance, and (ii) the switching or coupling factor. In current CMOS technologies the total capacitance is estimated as the sum of four components: (i) line-to-ground capacitance, (ii) coupling or lateral capacitance (between two nets on the same layers), (iii) parallel or crossover capacitance (due to overlap area of two nets on different layers), and (iv) fringing capacitance (formed between the edge of one conductor and the surface of another conductor on different layers) [41]-[44]. The total capacitance of a certain conductor (for example conductor-1 in Fig.6.2) in a multi-layer representation is given by

\[ C_{total} = C_{gnd} + C_l + C_p + C_f \]  

(6.1)

Fig.6.2 Capacitances of a conductor in a multi-layer representation
Due to the recent trends of technology scaling, the ratio between the coupling or lateral capacitance to the total capacitance is increasing (see Fig. 6.3 [50], [53]). The coupling capacitance ($C_l$) is becoming stronger due to the decrease of spacing between conducting lines, the increase of interconnect length and aspect ratio, and the longer overlap area among lines in the same layers [41]-[53], [108]-[110]. This is particularly true in the upper metal layers, where power and clock distribution networks, and global signal lines run across the whole chip area. Bus-dominant design worsens the effects of coupling, since it results in longer parallel wires. This growing coupling can affect circuit operation severely depending on the switching or coupling factor. Since most lines have two parallel neighboring lines on two sides, the total coupling factor for a line is in the range
of zero to four [32], [54]. In the worst case the coupling factor is 4.

Most of the previous work treated the noise immunity and the noise content separately, and emphasized the fact that noise immunity of CMOS digital integrated circuits degrades with the scaling of technology. However, it is important to note that the noise content in dynamic circuit decreases with the scaling down of supply voltage. Moreover, with the increase of clock frequency, the injected noise in a dynamic circuit will have less time to disrupt (charge or discharge) the capacitor holding the logic level at the dynamic node. This time is typically half a clock cycle for symmetric clocks. As a result dynamic circuits can tolerate higher noise at higher frequencies. Therefore, while the overall trends of modern CMOS technology make CMOS digital circuits more susceptible to noise, decreasing supply voltage and increasing frequency actually have positive effects on the noise tolerance of dynamic circuits. Consequently, a more realistic and positive analysis of noise scalability in dynamic circuit is imperative. This paper focuses on the coupling noise issues in dynamic circuits. The rest of the paper is organized as follows. Section 6.2 presents a simple and accurate formula to calculate the induced noise voltage on a dynamic node due to coupling. Section 6.3 presents closed form analytical solutions for noise tolerance metrics for dynamic circuits. Section 6.4 introduces a positive analysis of noise in dynamic circuit and presents the idea of realistic noise scalability with technology scaling. Section 6.5 concludes the paper.
6.2. Noise Voltage at Dynamic Node Due to Coupling

As coupling becomes stronger, the noise content injected into a dynamic circuit through coupling is increasing. The magnitude of the induced noise voltage on the dynamic victim node $N$ (see Fig. 6.4) due to switching of the aggressor net depends on the ratio of the total effective coupling capacitance ($C_{CT}$) to the total capacitance of the victim net ($C_{TOTAL} = C_{CT} + C_{GT}$).

![Diagram of Coupling of a dynamic net]

Here $C_{GT}$ includes all the components of capacitance of the victim net except the lateral or coupling capacitance. When the victim net is quiet and the aggressor net is switching from low to high, the magnitude of the induced noise voltage ($\Delta V$) on the dynamic victim node can be given by simple voltage divider formula (6.2).

$$\Delta V = \frac{C_{CT}}{C_{CT} + C_{GT}} \cdot \frac{V_{dd}}{V_{dd}} = \frac{C_{CT}}{C_{TOTAL}} \cdot V_{dd}$$  \hspace{1cm} (6.2)
SPICE simulations (Table 6.1) of three pairs of coupled interconnect lines with increasing $C_{CT}/C_{TOTAL}$ ratios give exactly the same results as equation (6.2). It is observed from (6.2) as well as from the simulations that for a certain $V_{dd}$ the magnitude of the induced noise $\Delta V$ linearly increases with the $C_{CT}/C_{TOTAL}$ ratio.

<table>
<thead>
<tr>
<th>$C_{CT}/C_{TOTAL}$</th>
<th>0.36</th>
<th>0.41</th>
<th>0.45</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$ (volts)</td>
<td>3</td>
<td>1.8</td>
<td>1.08</td>
</tr>
<tr>
<td>$\Delta V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulation</td>
<td>1.06</td>
<td>0.635</td>
<td>0.38</td>
</tr>
<tr>
<td>Eqn. (6.2)</td>
<td>1.07</td>
<td>0.64</td>
<td>0.386</td>
</tr>
</tbody>
</table>

It is important to note that the self and mutual inductances won’t affect the final magnitude of the injected noise voltage $\Delta V$. Inductances will contribute some initial overshoots and oscillations, but the final value of $\Delta V$ depends purely on the ratio $C_{CT}/C_{TOTAL}$ (see Fig.6.5). Also increasing frequency won’t have any effect on the final magnitude of the noise voltage $\Delta V$. At higher frequency the final value of $\Delta V$ will be reached faster.
6.2: Noise Voltage at Dynamic Node Due to Coupling

Fig. 6.5. Effects of inductances on the noise level
6.3. Noise Tolerance Metrics for Dynamic Circuits

If the victim net of Fig.6.4 drives a dynamic circuit (see Fig. 6.6), the induced noise voltage $\Delta V$ will propagate through the dynamic circuit and affect the operation of the driven circuit depending on the magnitude and the direction of $\Delta V$. Consider the case when $V_{out}$ is precharged to $V_{dd}$. In the evaluation mode (with $\phi = \text{“1”}$ and $V_{in} = \text{“0”}$), if $\Delta V$ lowers the victim net voltage below “0”, it will cause bootstrapping in the driven circuit.

If $\Delta V$ raises the victim net voltage above $V_{tn}$, the PDN network turns ON, and $V_{out}$ starts to discharge. In this case, the PDN is assumed to be a single NMOS transistor such as in a
NOR gate, which represents a worst-case noise effect. Using the $\alpha$-power law model [56] for the devices, the discharge current can be given by

$$I = I_1 = I_2$$  \hspace{1cm} (6.3)

where,

$$I_1 = p_c (\Delta V - V_e - V_m)^\alpha$$  \hspace{1cm} (6.4)

$$I_2 = \frac{p_c}{p_v} (\varphi - V_m)^{\alpha/2} V_e$$  \hspace{1cm} (6.5)

Here $\alpha$ is the velocity saturation constant; $p_c$ and $p_v$ are the constants that characterize the current drive capability of the transistor in the saturation and in the linear region, respectively. Here the clock signal $\varphi = V_{dd}$. Iteratively solving (6.3), (6.4) and (6.5) we get the expression (6.6) for the discharge current as a function of $\Delta V$.

$$I = p_c (\Delta V - V_e - V_m)^\alpha$$  \hspace{1cm} (6.6)

where $V_e = p_v \left[ \frac{\Delta V - V_e - V_m}{(V_{dd} - V_m)^{\alpha/2}} \right]^\alpha$ and $V_{el} = \frac{\Delta V - V_m}{1 + \frac{1}{p_v} (V_{dd} - V_m)^{\alpha/2}}$. In this iterative solution of $V_e$ to calculate discharge current $I$, we made an initial guess of $\alpha = 1$, which is a good approximation for deep submicron circuits.
It is clear from (6.6) that the discharge current $I$ increase almost linearly with $\Delta V$.

Simulation results (see Fig. 6.7) for MOSIS TSMC 0.18µm technology also reveal the fact that higher noise voltage $\Delta V$ on the victim net results in faster discharge of the...
dynamic output node voltage of the driven circuit. Since the discharge current is constant at a certain level of $\Delta V$ over the time of interest (see Fig. 6.7), the change of the output voltage with time can be given by

$$V_{out}(t) = V_{dd} - \frac{I \cdot t}{C_L}$$  \hfill (6.7)

Here the magnitude of the output voltage change ($\frac{I \cdot t}{C_L}$) is directly proportional to the discharge current ($I$), which is a function of $\Delta V$. Therefore, with the increase of $\Delta V$ the output voltage falls further below the correct logic level (which is $V_{dd}$ in this case). If $\frac{I \cdot t}{C_L}$ becomes equal to or greater than $NM_H$ of the dynamic circuit, eventually a functional failure occurs. The magnitude of the output voltage change is time dependent. For a certain level of $\Delta V$, the discharge current will remain for a shorter period of time with smaller clock cycle. To investigate when a circuit will fail for a certain noise level, consider that the circuit will fail at $V_{out}(t) = qV_{dd}$, where the multiplying factor $q$ is in the range [0-1], which depends on the noise margins. For an ideal inverter, which has a switching threshold of $\frac{V_{dd}}{2}$, the value of $q$ is 0.5. Higher value of $q$ means lower noise margin or larger factor of safety. From (6.7) we get

$$t = \frac{V_{dd} - V_{out}(t)}{I} \cdot C_L$$  \hfill (6.8)
Therefore, the time for a dynamic circuit to fail can be given by

\[ t_{\text{failure}} = \frac{(1 - q) V_{dd}}{I} C_L \]  (6.9)

From (6.6) and (6.9) it can be inferred that with higher \( \Delta V \) (higher \( I \)), the dynamic circuit will fail quickly, and with smaller cycle time the circuit can tolerate higher \( \Delta V \) without functional failure. Therefore for a circuit to operate without any functional failure due to noise, the limit on the clock cycle time is (assuming a symmetric clock)

\[ t_{\text{cycle}} < 2 \cdot t_{\text{failure}} \]  (6.10)

For a certain \( \Delta V \), the dynamic output voltage will be discharged below the noise margin and a logic error will occur when

\[ t_{\text{cycle}} \geq 2 \cdot t_{\text{failure}} \]  (6.11)

By plotting \( t_{\text{cycle}} = 2 \cdot t_{\text{failure}} \) as function of \( \Delta V \) we can define an area of safe operation for the dynamic circuit (see Fig. 6.8 for TSMC 0.18\( \mu \)m technology). Here we consider \( q = 0.7 \). That is, noise margin \( NM_H = 0.3 V_{dd} \).

For reliable operation the operating point of the dynamic circuit must be lower than the \( \Delta V \)-\( t_{\text{cycle}} \) curve in Fig. 6.8. For example, with \( \Delta V = 0.6 \text{ volts} \) the circuit of Fig. 6.6 will have a functional failure with a clock cycle of 0.81ns or higher, and the corresponding time at which \( V_{\text{out}} \) falls below \( qV_{dd} \) (1.26 volts) is 0.405ns. Dynamic simulations (Table 6.2 and Fig. 6.9) give the same results with very low margin of error. From Fig. 6.9 it is observed that as the noise level increases from 0.6volts to 1.0volts, the functional failure
time for the dynamic circuit decreases from 0.409ns to 0.172ns. The calculation error between the expression and the simulation is higher at lower noise level, but it is not that significant since at lower noise level there is less possibility of functional error. The proposed expressions are more accurate at higher $\Delta V$, which is the region of most interest.

![Graph showing output voltage over time for different noise levels](image)

### Table 6.2: Failure time at different noise voltage ($q = 0.7$)

<table>
<thead>
<tr>
<th>$\Delta V$ (volts)</th>
<th>Analytical value $t_{failure}$</th>
<th>Simulation $t_{failure}$</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>0.93ns</td>
<td>0.845ns</td>
<td>10</td>
</tr>
<tr>
<td>0.6</td>
<td>0.405ns</td>
<td>0.409ns</td>
<td>1</td>
</tr>
<tr>
<td>0.8</td>
<td>0.245ns</td>
<td>0.249ns</td>
<td>1.6</td>
</tr>
<tr>
<td>1.0</td>
<td>0.170ns</td>
<td>0.172ns</td>
<td>1.2</td>
</tr>
</tbody>
</table>

![Functional failure at different levels of noise](image)

**Fig. 6.9** Functional failure at different levels of noise
Dynamic circuits are often protected by keeper transistors, which regenerate logic states of noise-affected evaluation nodes by weak feedback. Here the analysis of noise tolerance metrics for dynamic circuits has been performed without the keeper transistor for two reasons. The design of the latch transistors in keeper technique is ratioed, and the feedback transistors are sized so that it will supply enough current to cancel the effects of noise with a sacrifice of performance, such as, reduced speed, increased area, and increased power consumption. This transistor is not very fast, since the size of this transistor is kept as small as possible to limit the performance degradation. Consequently, discharge current due to large noise at the input of the PDN network can bring down the output voltage level before the weak feedback transistor can restore the logic level. Again, if the designers’ goal is to make dynamic circuits robust against noise disturbance by utilizing keeper logic technique, the analysis of noise tolerance metrics of unguarded dynamic circuits will help to properly size the restoring feedback transistor.
6.4. Noise Scalability

Coupling is becoming stronger with technology scaling, and this stronger coupling is leading to higher noise injection, thereby degrading noise tolerance of CMOS digital integrated circuits. Most of the work in this area analyzed the noise effects from this conservative approach. This paper, however, emphasizes two important observations about noise scalability in dynamic circuits. While the overall scaling trends are making CMOS digital circuits more susceptible to noise, there are two positive trends that actually help improve noise tolerance in dynamic circuits. Equation (6.2) shows that the induced noise voltage is linearly dependent on the supply voltage \( V_{dd} \), which is scaling down. Therefore, for a certain ratio of \( C_{CT}/C_{TOTAL} \), the magnitude of the noise voltage will be decreased linearly with the supply voltage. In that sense, higher noise content due to increasing \( C_{CT}/C_{TOTAL} \) ratio can be counter balanced by decreasing supply voltage.

![Fig. 6.10 Improving noise tolerance with increasing frequency](image)

Fig. 6.10 Improving noise tolerance with increasing frequency
Second, since the frequency of CMOS technologies is continuously increasing, the available time to disrupt the logic level of any dynamic node is decreasing. So the output voltage change \( \frac{I_d}{C_L} \) due to a certain noise voltage \( \Delta V \) will be less at higher frequencies. Dynamic simulations (see Fig. 6.10) of the above example circuit with a constant \( \Delta V = 1.0 \) volts at three different frequencies show that the output voltage drop is lower at lower \( t_{cycle} \). Therefore, noise tolerance of a dynamic circuit tends to improve with the increase of frequency, since a dynamic node can tolerate higher noise without functional failure as the cycle time goes down.

The static noise margin is a conservative measure of noise immunity for dynamic circuit, since the noise amplitude can safely be higher than threshold voltage at a lower clock cycle time, and noise content itself is lower at lower supply voltage. In addition the static approach ignores the fact that logic gates also acts as low-pass filters [36]. Therefore, adhering to the static noise margin could severely restrict the performance of a dynamic circuit. Since \( V_{dd} \) is scaling down by \( 1/s \) in current CMOS technologies, the noise content \( \Delta V \) can be lowered if the \( C_{CT}/C_{TOTAL} \) ratio can be kept constant or scales up by a factor less than technology scaling factor \( s \). Lowering the noise content is important, since load capacitance is being scaled down with technology scaling. At the same time the scaling down of \( V_{tn} \) by \( 1/s \) decreases noise margins by \( 1/s \). Consequently, noises with shorter duration and smaller amplitude can cause logic failure. The negative effects of reduced load capacitance and smaller noise margins can be counter balanced to some
extent by the increase of frequency by $s$, since higher frequency means less time to charge or discharge the capacitance responsible for holding logic level. Based on the above observations and assumptions, it can be inferred that noise in dynamic circuit can be made scalable to some degree.

Here the analysis is presented based on the growing coupling between interconnect lines. However, it is important to consider various other factors, e.g., faster aggressor transition times, increased leakage current, process variations. Our future work will attempt to address these issues together with increasing coupling for comprehensive study of scalability of noise in dynamic circuits.
6.5. Conclusion

Considering the increasing popularity of dynamic circuits, and the growing level of coupling between wires, this paper explored the issues of coupling noise in dynamic circuits. The proposed analytical solutions for noise as well as noise tolerance metrics closely estimate the behavior of a dynamic circuit under the influence of coupling noise. The analytical expressions give results with around 5% margin of error. A more realistic approach is presented as compared to the conservative approach towards noise immunity. It is shown that to some degree noise can be made scalable with technology due to the linear dependency of noise level on the supply voltage and the $C_{CT}/C_{TOTAL}$ ratio. It is also illustrated that increasing frequency improves noise tolerance by allowing dynamic circuits to tolerate higher noise levels.
Chapter 7: Possible Noise Failure Modes in Static and Dynamic Circuits

Injection of noise causes temporary or permanent signal deviation on a circuit node depending on the level of noise and the affected circuit. The deviation of signal level of the circuit node may lead to functional failure in digital circuits, particularly in dynamic circuit families. Static circuits are inherently robust and can effectively restore the signal deviation before having undesired logic shift. However, some static circuits with a feedback loop cannot recover from noise-induced errors. This chapter investigates possible failure modes in both dynamic and static CMOS digital circuits due to noise disturbance. In current VLSI circuits, where mixture of static and dynamic implementation is very common, it is important to identify possible noise failure modes to help that designers develop techniques to prevent such failures. This chapter also illustrates the observation that increasing frequency may lead to higher probability of logic failure due to noise.
7.1 Introduction

With continuous scaling of feature sizes in deep submicron digital VLSI technologies, noise effects are having significant impact on circuit performance and signal integrity [27]-[53]. A general CMOS circuit has input signals, output signals, internal static and dynamic nodes, and power and ground nodes on which noise can be injected from the various sources. Noise sources, that are most relevant to CMOS digital circuits, are (i) charge leakage and substrate noise, (ii) charge sharing noise, (iii) power and ground supply noise, and (iv) coupling or crosstalk noise [27]-[36]. With scaling of technology into the nano-meter regime the crosstalk due to capacitive and inductive coupling between neighboring lines is increasing, which makes circuit more prone to noise disturbance [50]-[55].

Whatever the sources or types of noise, the injection of noise into a circuit node causes a signal deviation at that node. This deviation of signal will affect the operation of the circuit or circuit block driven by the victim net, and may lead to different kinds of unexpected behavior including functional failure or logic error. A functional failure is possible when an induced noise is propagated and wrongly evaluated at the primary output. The parameters that determine if there will be a logic error are (i) the amplitude and the duration of the noise pulse, (ii) the type of the victim node and the circuit connected to the victim node, and (iii) the signal condition on the affected node. In static circuits momentary deviation of logic levels can be restored automatically, since at steady
state the nodes are always connected either to ground or $V_{dd}$. But this restoration is not possible in dynamic circuits due to the possibility of having floating nodes [36], [55]. As a result the duration of the signal deviation may be equal to the length of clock pulse for dynamic circuits. However, in case of static circuits the signal deviation is always in the form of a glitch or a pulse with a small duration $\Delta t$ (as illustrated in Fig.6.1). Consequently, dynamic circuits are more likely to suffer logic error due to noise disturbance. The worst-case scenario is when a dynamic victim node drives a dynamic gate. As opposed to dynamic circuits, static circuits are less likely to suffer from logic failure. However, static latches like $D$ flip-flops have a feedback loop that cannot recover from noise-induced errors.

![Diagram](image.png)

Fig.7.1. Effect of Noise on Static and Dynamic Node
Since current CMOS digital designs can have a mixture of dynamic and static implementation in the same circuit, there may be many possible modes for logic failure. Circuits may change state at some signal switching conditions depending on the incoming noise level, shape, and duration. Since the impact of noise is becoming critical with scaling trends, it is important to detect possible modes of logic or functional failure in different circuit families. The rest of the chapter is organized as follows. Section 7.2 of this chapter examines the modes of logic failure in combinational circuit families. Section 7.3 explores the possibility of logic failure in sequential circuits. Section 7.4 introduces an observation about increasing frequency and it’s effects on the probability of logic failure due to noise. Finally section 7.5 concludes the chapter.
7.2 Failures in Combinational Circuits

7.2.1 Noise Failures in Dynamic Combinational Circuits

Dynamic gates are more prone to logic failure due to noise, since its DC noise margin can be as low as the threshold voltage of the pull-down transistors. The failure due to noise at the input of dynamic gate occurs when the signal deviation of the input victim net exceeds the DC noise margins of the following gate. If the victim net in Fig. 6.1 drives a dynamic circuit (e.g. a dynamic inverter as in Fig. 7.2) the injected noise ($V_{\text{noise}}$) will propagate through the dynamic circuit and affect its operation depending on the magnitude and the direction of $V_{\text{noise}}$. Two cases are considered: (i) victim node $N$ is dynamic, and (ii) victim node $N$ is static.

![Diagram of a dynamic inverter driven by a noise-affected line](image)

Fig. 7.2 A dynamic inverter driven by a noise-affected line
In case of a dynamic victim node the duration of noise voltage $V_{\text{noise}}$ is equal to the clock period. If the dynamic inverter in Fig.7.2 is pre-charged to $V_{dd}$ and the magnitude of $V_{\text{noise}}$ is slightly greater than the threshold voltage $V_{tn}$ of the transistor $M_n$, the transistor $M_n$ turns ON, and $V_{out}$ starts to discharge. Analytical solution as in (6.6) [55] and simulation (see Fig.7.3 [55]) reveal that the discharge current $I$ (where $I = I_1 = I_2$) depends almost linearly on the level of induced noise voltage $V_{\text{noise}}$.

$$I = p_c \left( V_{\text{noise}} - V_e - V_{tn} \right)^\alpha$$

(7.1)

where $V_e = p_v \left[ \frac{V_{\text{noise}} - V_{el} - V_{tn}}{(V_{dd} - V_{tn})^{1/2}} \right]^\alpha$ and $V_{el} = \frac{V_{\text{noise}} - V_{tn}}{1 + \frac{1}{p_v} (V_{dd} - V_{tn})^{1/2}}$. Here $\alpha$ is the velocity saturation constant; $p_c$ is the constant that characterize the current drive capability of the transistor in the saturation region.

Fig.7.3 Discharge current $I$ as a function of $V_{\text{noise}}$ in a dynamic inverter driven by a dynamic victim net.
The time required to discharge \( V_{out} \) is given by

\[
t = \frac{V_{dd} - V_{out}(t)}{I} \cdot C_L
\]  

(7.2)

If the clock cycle is long enough to allow the discharge current \( I \) to bring down \( V_{out} \) below logic threshold, eventually there will be a functional failure (see Fig.7.4). Since the discharge current \( I \) depend almost linearly on \( V_{noise} \), the circuit will have functional failure faster at higher level of \( V_{noise} \). However, if the clock frequency of the driven dynamic circuit is very high so that the discharge current cannot sustain long enough to bring down \( V_{out} \) beyond the logic threshold, then higher level of \( V_{noise} \) can be tolerated without functional failure. Therefore, while a higher level of \( V_{noise} \) leads to faster functional failure of the driven dynamic circuit, higher frequency enables to tolerate higher \( V_{noise} \) by a dynamic circuit.

Now if the input victim net of Fig.7.2 is static, the discharge current stops as soon as the injected noise pulse disappears. Since the duration of the noise pulse on the static victim is a small fraction of the clock cycle, the effect will not be as severe as that of dynamic input victim net. Fig.7.5 shows that with a noise pulse of duration 0.5ns, having same amplitude as before, the change of \( V_{out} \) is much less than in the case of Fig.7.4. It is important to note that in both cases the deviation of the signal level of the driven dynamic circuit cannot be restored to the original level although the effect in case of a static victim net is much less than the case of a dynamic victim net. Therefore the dynamic-dynamic combination is likely to have higher possibility of logic error than the static-dynamic combination.
combination. Noise pulses with higher amplitude and width on a static victim net may lead to a logic failure in the driven dynamic circuit.

Fig. 7.4 Signal deviation of a dynamic circuit driven by dynamic victim net

Fig. 7.5 Signal deviation of a dynamic circuit driven by static victim net
7.2.2 Noise Failures in Static Combinational Circuits

Due to the inherent robustness of static combinational circuits, the possibility of having functional or logic error by noise disturbance is very low. Since every static circuit node is always connected to either ground or $V_{dd}$, any signal deviation caused by the injected noise is restored quickly. To have a logic shift in such a node both the amplitude and the duration of the induced noise voltage have to be very large, which is very rare. If the same victim net as in Fig.7.2 drives a static inverter (see Fig.7.6), the deviation of $V_{out}$ will be insignificant for the same noise contents compared to the cases of the dynamic inverter.

![Fig.7.6: A static combinational circuit driven by a noise-affected line.](image)
If the driving victim net is dynamic in nature, for the same noise content as in Fig.7.4, the deviation of $V_{out}$ is very small, and $V_{out}$ settles at a level slightly lower than $V_{dd}$ for the whole clock cycle (see Fig.7.7). If the noise content is higher than the switching threshold of the driven static circuit, there may be a chance of logic failure. However, noise content in that case has to be much greater than the noise content in Fig.7.4 for the dynamic circuit. If the driving victim net is static in nature the change of $V_{out}$ will be very small and temporary for the same noise content (see Fig.7.8). This transient deviation vanishes quickly and $V_{out}$ is restored to $V_{dd}$.

Fig.7.7 Signal deviation of a combinational static circuit driven by dynamic victim net
7.2.2: Noise Failures in Static Combinational Circuits

Fig. 7.8 Signal deviation of a combinational static circuit driven by static victim net

The above analysis supports the fact that for static combinational circuits, the probability of having logic failure due to noise disturbance is extremely low as compared to dynamic combinational circuits.
7.3 Logic Failure in Sequential Circuits

7.3.1 Noise Failures in Static Sequential Circuits

The main advantage of static logic over dynamic logic is its robustness under the influence of noise. But static logic may also suffer from logic failure if there is a feedback loop. Static D flip-flop (as in Fig.7.9), which are very common in registers, has a feedback loop that cannot recover from noise-induced errors. In these types of circuits there are three possible points where noise can be injected, which are the input, the clock and the feedback loop. Among these three points the feedback loop is the most sensitive to noise. Even a small noise pulse on the feedback loop when the clock is falling or inactive will be propagated repeatedly through the loop and may ultimately destroy the logic information stored in the flip-flop (see Fig.7.10). Fig.7.10 shows an unexpected shift of the logic levels of the D flip-flop in Fig.7.9 for a noise pulse of amplitude 0.9 volts and duration 0.2 ns.
Fig. 7.9 A simple D Flip-Flop: a common building block of register and storage unit.

Fig. 7.10: Functional failure in static D-latch. (a) Latch voltages at normal condition, (b) Logic error due to a small noise pulse of amplitude 0.9v and width 0.2ns.
7.3.2 Noise Failures in Dynamic Sequential Circuits

In case of static latches the clock and the input are not that sensitive to noise as compared to the feedback loop. However, for dynamic latches both the clock and the input may become vulnerable to noise at different signal and switching conditions of the latches. For the two examples of dynamic latches in Fig.7.11, there is a very high probability of logic failure due to noise at the clock and the input lines. If the input $D$ of the latch in Fig.7.11a switches from high to low after the fall of clock $\Phi$ the output $Q$ will be dynamic high at normal operating condition (see Fig.7.12a). At this stage a small positive noise pulse on the clock line due to coupling with the aggressor net will change the logic state, and $Q$ will be switched to “0” (see Fig.7.12b).

![Fig.7.11 Two different versions of dynamic N latch [27]](image_url)
7.3.2: Noise Failures in Dynamic Sequential Circuits

Fig. 7.12: Noise sensitivity of dynamic latches. (a) Normal operating condition, (b) With a small noise pulse of amplitude 0.9v and width 0.2ns

Similarly if the input $D$ of the same latch in Fig. 7.11a switches from low to high after the fall of clock ($\phi$) the output $Q$ will be dynamic low. At this stage a small positive noise pulse on the clock line will change the logic state, and $Q$ will be switched to “1”.

![Diagram](image)
For the latch in Fig.7.11b the output $Q$ is $V_{dd}$ when $D = "1"$ and $\Phi = "1"$. If the input $D$ falls after the fall of the clock $\Phi$ the output $Q$ should still be dynamic high as illustrated in Fig.7.12a. A small positive noise pulse on the clock signal line from aggressor net will cause logic failure as in Fig.7.12b. Again if the $D$ falls while the clock is high the output still should be dynamic high. A positive noise pulse on the low input may bring down the pre-charged output node $Q$. Although the input $D$ of the latch in Fig.7.11b is sensitive to noise, its sensitivity is less than the clock.

Fig.7.13 Comparison of noise immunity among three types of latch

Three noise immunity curves are presented in Fig.7.13 for the static D latches in Fig.7.9 and the two dynamic latches of Fig.7.11. Fig.7.13 plots the relative noise duration ($D_r$) against the relative noise amplitude ($A_r$). For the static D flip-flop noise pulses of various amplitudes and durations have been injected into the feedback loop, while
7.3.2: Noise Failures in Dynamic Sequential Circuits

keeping $V_{dd}$ constant. For the dynamic latches the noise immunity curves are for noise on the clock. SPICE simulations were used to determine the set of noise amplitudes and durations that cause an undesired logic shift. The area above each curve in Fig.7.13 represents the amplitudes and durations of a noise pulse that can cause logic failure. The relative noise amplitude is defined as $A_r = A/V_{dd}$, where $A$ is the amplitude of the noise pulse, and the relative duration of noise $D_r = D/C_f$, where $D$ is the duration of the noise pulse and $C_f$ is the cycle time. By comparing the noise immunity curves in Fig.7.13, it can be observed that dynamic latches are much more sensitive to noise than static latch.
7.4 Effect of Increasing Frequency on the Possibility of Logic Error due to Noise

It is important to note that with increasing clock frequencies, a circuit node may suffer from reduced voltage swing. That is, higher clock rate limits the achievable voltage swing at a circuit node (see Fig. 7.14), since there is not enough time to fully charge or discharge the load capacitance. \( C_f \) in Fig. 7.14 is clock cycle time required to obtain the full voltage swing \( V_{fs} \) from zero to \( V_{dd} \). Note that the supply voltage is not scaled here and is kept constant at \( V_{dd} \).

![Fig.7.14 Voltage at a circuit node at two different frequencies](image)

Fig. 7.14 illustrates the decrease of voltage swing \( V_s \) with the decrease of clock cycle time \( C \). The clock cycle time and the voltage swing are normalized against the clock.
cycle at full swing \((C_{fs})\) and the full swing voltage \((V_{fs})\), respectively. The relative voltage swing is defined as \(V_{sr} = V_s/V_{fs}\) and the relative cycle time \(C_r = C/C_{fs}\). If the voltage swings changes all the signals become faster by the same ratio independent of the capacitive load at a circuit node. From the shape of this curve it is important to notice that the change of voltage swing slows down at longer clock cycle time. This shape correctly maps the change of actual signals on-chip with time. Any signal at a circuit node rises quickly at the beginning and as the signal reaches close to the full swing value it takes longer time for a certain change. Therefore, to reach higher voltage swings, the cycle time significantly increases. The curve in Fig.7.15 has been produced by simulating a chain of gates driven by an inverter at different frequencies with constant supply voltage \(V_{dd}\).

Fig.7.15 Decrease of voltage swing with the increase of frequency
With a reduced signal level, a circuit node is more likely to suffer from logic failure due to a certain level of noise. Therefore, increasing frequency leads to higher probability of logic failure at a circuit node due to reduced voltage swing. A set of noise immunity curves for the \( D \) flip-flop in Fig.7.9 is presented in Fig.7.16, which plots the relative noise duration \( (D_r) \) against the relative noise amplitude \( (A_r) \) at various voltage swings. Noise pulses of various amplitudes and durations have been injected into the feedback loop of a \( D \) flip-flop at different voltage swings, while keeping \( V_{dd} \) constant. The area above each curve in Fig.7.16 represents the amplitudes and durations of a noise pulse that can cause logic failure at a certain voltage swing. Hence, the lower the voltage swing the larger the area of noise amplitudes and durations that can cause an error. The highest curve is for the full voltage swing \( V_{fs} \) (swing from zero to \( V_{dd} \)). The lower curves illustrate noise immunity at voltage swings smaller than the full swing. The relative cycle time \( C_r \) is always less than 1 for lower voltage swings.

Fig.7.17 plots the relative area above the noise immunity curve against the relative voltage swings \( (V_{rs}) \). It is observed that the area above the noise immunity curve increases with the decrease of the voltage swing, which means lower voltage swing leads to higher probability of logic error. The relation between cycle time and the area above the noise immunity curve in Fig.7.18 has been obtained by omitting the voltage swing variable from the two relations; cycle time versus voltage swing (Fig.7.15) and relative area above noise immunity curve versus voltage swing (Fig.7.17). The curve in Fig.7.18,
7.4: Effect of Increasing Frequency on the Possibility of Logic Error due to Noise

illustrates that higher frequency (smaller cycle time) leads to higher probability of logic error due to noise.

Fig.7.16 Noise immunity curves of a D flip-flop at various voltage swing

Fig.7.17 Relative area above noise immunity curve at various voltage swings
Fig. 7.18 Probability of error at different cycle time

Chapter 7: Possible Noise Failure Modes in Static and Dynamic Circuits
7.5 Conclusion

This paper explores various scenarios, when signal deviation due to noise can cause logic failure in both dynamic and static circuits. Effects of noise on logic integrity are investigated for both combinational and sequential circuit families. As expected, it is shown that both combinational and sequential dynamic circuit families are much more vulnerable to noise disturbance compared to their static counterparts. Although static circuits are considered very robust against noise disturbance, it is shown that static circuit with a feedback loop may suffer from logic failure at certain situations. It has been observed that a circuit node may suffer from reduced voltage swing at higher frequencies, simply because, higher clock rate limits time to fully charge or discharge the load capacitance responsible for holding logic level at a circuit node. At a reduced voltage swing a circuit node is more liable to logic failure due to a certain level of noise. Therefore, this paper also illustrates the observation that increasing frequency may lead to higher probability of logic failure due to noise.
Chapter 8 : Future Research

The advances in current deep submicron integrated circuit technologies have been following a scaling trend some time faster than Moore’s Law, leading to billion transistors integrated on a single chip. However, the gap between the super-linear progresses in integrated circuit technologies and the utilization of this enormous computing power is increasing due to various issues and challenges arising at every generation of technology. Future research must address these issues and try to decrease the gap. This chapter presents some of the critical issues and anticipated research objectives to address those issues.

The increasing importance of the electromagnetic properties of interconnect on the overall electrical performance of state-of-the-art very large scale integration (VLSI) systems; can be attributed to the rapid growth of the circuit complexities and frequencies. Therefore, the electrical modeling and analysis of the interconnect structure need to be extended to incorporate the issues regarding electrostatic as well as electromagnetic coupling. With switching speeds well below 1 ns, and VLSI circuit complexity exceeding the 100 million transistors per chip, power and signal distribution is characterized by multi gigahertz bandwidth pulses propagating through a tightly coupled three-dimensional wiring structure that exhibits resonant behavior at the upper part of the spectrum. Consequently, in addition to the inductive and capacitive coupling, present between adjacent wires across the entire frequency bandwidth, distributed
electromagnetic effects, manifested as interconnect-induced delay, reflection, radiation, and long-range non-local coupling, become prominent at high frequencies, with a decisive impact on the overall system performance. The electromagnetic nature of such high-frequency effects, combined with the geometric complexity of the interconnect structure; makes the electrical design of today’s performance-driven systems extremely challenging. Its success is heavily dependent on the availability of sophisticated electromagnetic modeling methodologies and computer-aided design tools. In this new scenario extensive research and studies are required to address issues regarding signal integrity, power management, timing performance, and various other unforeseen performance metrics. The next few sections illustrate some of future research objectives.
8.1 Delay Uncertainty due to Increasing Capacitive and Inductive Coupling of Interconnect Lines

Signal integrity is one of most critical issues in the gap between continuous advances and utilizations of current deep submicron and anticipated upcoming nano technologies. Among the various sources leading to severe signal integrity problems, coupling or crosstalk between interconnect lines is one of the dominant problems because it can cause functional as well as delay failure. With the increase of coupling between the high aspect ratio wires, the delay uncertainty is becoming very high in the current design flow. Analysis of delay uncertainty due to increasing coupling is critical to fulfill the timing constraints, avoid delay failure, and select and design a proper clocking scheme. The effective coupling, and the delay induced by coupling depend on the switching activity of neighboring lines. It is hard to predict the delay uncertainty in the presence of strong coupling, because the crosstalk induced delay is a complicated function of peak noise amplitude and duration, and the relative signal slew of the victim and the aggressor lines. Again the conflicting impact of capacitive and inductive coupling on the delay characteristics of switching interconnect lines makes the prediction of delay uncertainty even more complicated. Future research must address all of these issues to identify possible challenges and issues regarding delay and timing performance, and to develop methodologies to overcome these challenges.
One of the most critical signals in a synchronous digital circuit is the clock signal. Controlling the clock signal delay in the presence of various noise sources, process parameter variations, and environmental effects represents a fundamental problem in the design of high-speed synchronous circuits. It is important to reduce the uncertainty of the clock signal delay, particularly of the clock signals driving the registers belonging to the most critical data paths.
8.2 Low Power Design and Power Management with Enhanced Noise and Leakage Current Level

As wireless networks and mobile accessories advance to support higher data rates and rich data/video applications, managing power consumption of future handheld devices is emerging as a top concern. Use of nanometer technologies enables progressively more system-on-chip integration and on-chip voltage scaling, thereby helping to reduce power consumption significantly. However, use of technologies 120nm and below will also severely enhance noise and leakage current levels, contributing to new power consumption sources, and challenging traditional ways of power management. Future research should focus on the emerging issues of power consumption, such as

- The challenges and opportunities imposed by deep sub-micron technology scaling, and increased noise and leakage current
- System-level and micro-architectural level techniques to manage/minimize power
- Design tools to address low power issues

In current CMOS technologies dynamic logic circuits are gaining popularity, since they provide very fast switching with modest area usage. They have been successfully used in several well-known chips and are the basis of DRAMs and other important computer components. Unfortunately, they can be power hungry which may limit their usage. In dynamic circuits, the clock period defines the ‘precharge’ and ‘evaluate’ operations in
every cycle. Since charge cannot be held on a capacitive node, every precharge cycle will pull current from the voltage source, adding to the overall power dissipation of the circuit. The clock circuits themselves require dynamic power to drive the FETs to the clock drivers corresponding to the precharge and evaluate transistors. The power consumption of the clock circuits alone can be a substantial portion of the total dissipated power.
8.3 Minimizing Capacitive and Inductive Coupling

There have been many techniques proposed to reduce coupling between adjacent lines in digital integrated circuits. Some of the commonly used techniques are increasing the width and the spacing of signal lines, passive and active shielding, buffer insertion, and differential signaling, etc. Most of these techniques handle capacitive coupling. Shielding is one of the most successful techniques to reduce capacitive coupling. Shields are nothing but ground and power lines placed between wires to prevent direct coupling between them. These power or ground lines are capable of screening signal lines and thus eliminating capacitive coupling. However, unlike coupling capacitance, which is a short-range phenomenon, inductive coupling can be a long-range phenomenon. Due to the long range of current return paths, traditional shielding, by inserting power/ground lines between signal lines, is capable of screening only part of these current return paths [23]. Besides, extensive shielding is not favorable, especially for dynamic circuits, due to the sacrifice of speed, the demands for high density, and relatively higher cost of wires in current processes.

Current trends of CMOS processes are making inductive coupling very significant. Inductive coupling can combine with capacitive coupling to cause severe noise in CMOS digital circuits. Increasing usage of noise-sensitive dynamic circuit is making noise worse than anticipated. There are not many significant methods proposed to reduce the effects of inductive coupling in static and dynamic circuits. As an improvement over traditional
shielding a new approach, called differential signaling, is proposed by [23] to handle inductive coupling. Another future research focus is to extend some of the existing techniques, and to develop new techniques for reducing both capacitive and inductive coupling in static as well as dynamic circuits.
8.4 Noise Tolerant Static and Dynamic Circuits

There has been significant focus on developing noise tolerant circuit design techniques due to the increasing prominence of signal integrity issues in deep submicron CMOS technologies. With the continuous changes in technology, older techniques often fail to offer the expected improvement in terms of noise tolerance without sacrificing considerable performance. In dynamic design, processes providing week feedback transistors - known as keeper transistors, are standard practice. But these transistors are sized so that it will supply enough current to cancel the effects of noise. The ratioed design of the feedback transistor is a serious drawback due to its static power consumption. This is a critical point with the continuous scaling down of supply voltages. Keeper transistors also increase the capacitive load for the driving gate, leading to speed penalty.

Increasing switching threshold is another effective way to improve noise tolerance of digital circuits. For domino logic, several techniques have been proposed to improve noise tolerance by increasing the switching threshold. But these techniques inevitably scarify circuit performance such as speed and power consumption, which are the most attractive aspects of dynamic circuits.

Any applicable noise tolerance improvement technique for dynamic circuits should provide substantial improvement with minimal performance penalty. New noise-tolerant circuit design techniques have to be developed for better performance in terms noise
immunity, robustness, and reliability together with energy efficiency, speed and area requirements. Another future objective of our future research is to develop noise-tolerant circuit techniques for both static and dynamic logic designs.
8.5 Developing Interconnect Centric CAD tools

In addition to the need for fundamental advances in circuit analysis and semiconductor process and materials, the explosive growth of integrated circuit complexity calls for a very sophisticated computer-aided design (CAD) approach to system architecture and circuit design. The electrical design of the supporting interconnect circuit is no exception. The interconnect-centric electrical CAD tools are the youngest members of the electrical design automation (EDA) framework used today for advanced VLSI design. They are also the most difficult to streamline and integrate into the design flow. One of the reasons for this is entirely physical. The electromagnetic field interactions they attempt to model are long-range, non-local, and strongly dependent on the electrical and geometric parameters of both the interconnect structure and the integrating substrates. The other reason is cultural. Circuit designers are taking advantage of the continuous reduction in feature size to pack more functionality in the chip rather than reduce its size. As the interconnect complexity escalates, its electrical design becomes more challenging. In fact, as is the case for most CAD tools, technologies continue to outpace the CAD tools that are being developed for interconnect electrical design. However, it is important to make significant progress to a turning point in this race, where the electromagnetic CAD tools will eventually be able to catch up with the technology advances and meet the design challenges.
Chapter 9 : Conclusion

Due to the continuous advances and scaling of CMOS digital integrated circuit technologies, interconnect parasitic elements have become dominant over gate parasitic elements in current deep submicron and anticipated future nanometer integrated circuit technologies. For very high performance integrated circuits, some of the signal lines need more accurate transmission line modeling, requiring the introduction of self and mutual inductances. It is shown that in analyzing VLSI circuit if standard distributed \( RC \) models are used ignoring inductive effects, large errors occur in the prediction and evaluation of the circuit behavior. It is observed that the self and mutual inductances affect deep submicron VLSI circuit performance by increasing signal propagation delay and oscillations, and decreasing rise time at any given input switching condition. A set of closed form expressions has been presented here to estimate integrated circuit behavior in the presence of self and mutual inductances. The expressions give results fairly close to simulation, and can be evaluated in a time comparable to Elmore delay. The approximate delay model has been used to intuitively understand some of the behavior of integrated circuits in the presence of self and mutual inductances. First, the delay model has been used to show that damping factor can be used as a figure of merit to characterize the importance of self and mutual inductances. On the basis of the approximations it is analytically shown that ground shielding is not very effective in minimizing inductive coupling, and differential bus switching scheme can give better coupling minimization as
compared to traditional shielding when inductive coupling is considered. Based on the model it is also shown, and supported by simulations that the delay uncertainty decreases as inductive effects increase.

With the increasing dominance of interconnect parasitics on integrated circuit performance, some signal lines are now modeled as distributed $RLC$ lines with coupling capacitance and mutual inductance for accurate analysis. Consequently, many commercial and proprietary extraction tools generate $RLCK$ circuits for high performance designs. Due to the large amount of data typically generated by extraction tools, significant run time and memory issues affect the analysis tools. Therefore, in the past decade there has been a significant focus to model the extracted netlist by a smaller model with minimal loss in accuracy. Most of these model order reduction methods produce reduced state-space or transfer function representations for the original extracted circuits. In order to take advantage of the model order reduction techniques, it is important to have a realizable netlist reduction method, i.e. $RLCK$ in – $RLCK$ out feature. Realizability is also important because this avoids the modification of mainstream analysis tools, since these tools are usually geared towards reading circuit netlists. Here a method for realizable reduction of extracted $RLCK$ netlists by node elimination has been presented. The method is much faster than model order reduction techniques and hence is appropriate as a pre-processing step. The proposed method eliminates nodes with time constants below a user specified time constant. By giving the freedom to the user to select
a critical point in the spectrum of nodal time constants, this method provides an option to make a tradeoff between accuracy and reduction. The proposed method preserves the DC characteristics and the first two moments at all nodes. It also recognizes and eliminates all the redundant inductances generated by the extraction tools.

With the continued scaling in modern deep submicron CMOS processes, signal integrity and noise has become an equally important metric to area, timing and power dissipation. The growing dominance of interconnects parasitic elements, such as, coupling capacitance and mutual inductance, is making the signal integrity issue increasingly critical. Performance requirements are driving designs in the direction of using noise-sensitive dynamic circuits, making the noise issues even more prominent. This work focuses on the trends of coupling and its effects on dynamic circuits. A set of closed form analytical solutions for noise as well as noise tolerance metrics for dynamic circuits has been presented. These solutions are within 5% of dynamic simulations. It is shown that not all scaling trends are negative for noise, and that the scaling down of supply voltage and increasing frequency help improve certain aspects of the noise immunity of dynamic circuit. Most of the work treated the noise immunity and the noise content separately. Here a more realistic approach is presented as compared to the conservative approach towards noise immunity by looking at the noise immunity and the noise content simultaneously. It is shown that to some degree noise can be made scalable with technology due to the linear dependency of noise level on the supply voltage and the
$C_{CT}/C_{TOTAL}$ ratio. It is also illustrated that increasing frequency improves noise tolerance by allowing dynamic circuits to tolerate higher noise levels.

Among the various sources of noise in current deep submicron CMOS technologies the noise due to capacitive and inductive coupling between neighboring interconnect lines has become dominant. Coupling noise imposes two serious side effects on digital integrated circuits. Coupling can cause the effective line capacitance and inductance to increase or decrease in the presence of simultaneously switching coupled lines, increasing or decreasing the signal delay. Second, it can cause functional failures by charging or discharging the capacitor responsible for holding the logic level at an evaluation node. Injection of noise causes temporary or permanent signal deviation on a circuit node depending on the level of noise and the affected circuit. The deviation of signal level of the circuit node may lead to functional failure in digital circuits, particularly in dynamic circuit families. Static circuits are inherently robust and can effectively restore the signal deviation before having undesired logic shift. However, some static circuits with a feedback loop cannot recover from noise-induced errors. Here various scenarios have been explored, when signal deviation due to noise can cause logic failure in both dynamic and static circuits. Effects of noise on logic integrity are investigated for both combinational and sequential circuit families. As expected, it is shown that both combinational and sequential dynamic circuit families are much more vulnerable to noise disturbance compared to their static counterparts. Although static
circuits are considered very robust against noise disturbance, it is shown that static circuit with a feedback loop may suffer from logic failure at certain situations. It has been observed that a circuit node may suffer from reduced voltage swing at higher frequencies, simply because, higher clock rate limits time to fully charge or discharge the load capacitance responsible for holding logic level at a circuit node. At a reduced voltage swing a circuit node is more liable to logic failure due to a certain level of noise. Therefore, it can be inferred that increasing frequency may lead to higher probability of logic failure due to noise.

In addition to the results and suggestions provided in the first few chapters, it is hoped that the work presented in this thesis provide a foundation for future research in the related fields of high performance integrated circuit analysis. At the present time, several other related areas of research suggest themselves, which were presented in the last chapter. Based on the presented results and analysis, it can be inferred that the proposed future extension to several dimensions is conceptually straightforward for deep submicron CMOS digital integrated circuits. However, as we enter into the nanometer regime the relative implications of these issues may take a different course. Future work must take this into account. It is also important to broaden these research from purely digital to mixed mode integrated circuit analysis. Most of these issues and analysis techniques can and must be extended in the context of System-On-a-Chip environment, which is going to be a mixed signal environment. It is also important to remember that to
find an acceptable solution of a particular issue of integrated circuit design, one cannot work independently in his or her own domain. Interaction with other groups of the same and different layers in the design hierarchy will help broaden one’s research domain and address any issue from wider perspective.
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Appendix A: Moments Calculation for Inductively and Capacitively Coupled $RLC$ Trees

![Image of an RLC interconnect network with capacitive and inductive coupling]

For any interconnect structure, if after removing the inductive and capacitive coupling all that remains is a set of $RLC$ trees and lines, this structure is considered a tree based structure. An example is the circuit in Fig.A.1, where if inductive and capacitive coupling are removed, a tree and two lines remain. For such capacitively and inductively coupled $RLC$ trees, the moments of the response at different nodes can be calculated in linear time.
using simple recursive formulae. Capacitively and inductively coupled trees have multiple inputs. The case is considered here when all the inputs have the same waveform shape but are not necessarily switching in the same direction. The waveform shape is arbitrary. For a node $i$ where the moments are being calculated, the input with a DC path to $i$ is called the primary input. For example, the primary input for node $i$ in Fig.A.1 is $V_{in2}$. $V_{in1}$ and $V_{in3}$ have no DC path to node $i$ since both capacitive and inductive coupling are open circuit at DC.

Consider calculating the moments at node $i$ of Fig.A.1, a capacitively and inductively coupled tree structure. The voltage at node $i$ can be expressed as

$$V_i(s) = V_{inp}(s) - \sum_l \left( R_k + sL_j \right) \sum_{r,j} C_{ri} s(V_r(s) - V_j(s)) - \sum_k sM_{lk} \sum_{l,m} C_{lm} s(V_l(s) - V_m(s))$$

where $k$ runs over all the branches on the path from the primary input to node $i$ on the tree, which $i$ belongs to; $r$ runs over all the nodes downstream of $k$ on that tree, and $j$ runs over all the nodes to which $r$ has a capacitance connected to. In the case of capacitances to ground, $j = 0$. $V_{inp}$ is the primary input for node $i$. For example, in Fig.A.1, there are two resistances, $R_3$ and $R_4$, from the primary input to node $i$. Hence, $k$ runs over $R_3$ and $R_4$, $L_3$ and $L_4$, and the mutual inductances $M_{13}$, $M_{36}$, and $M_{24}$. The index $l$ runs over all the nodes downstream of $M_k$ on the coupled tree (which $i$ does not belong to). The index $m$ runs over all the nodes which $l$ has a capacitance connected to.

The above formula can be understood by noting that the summations
represent the currents flowing out of nodes $k$ and $l$, respectively. The term

$$(R_k + sL_k) \sum_{r,j} C_{rj}s(V_r(s) - V_j(s))$$

(A.3)

in Fig.A.1 represents the voltage drop between the primary input and node $i$ due to the current flowing out of node $k$. Note that the node $k$ belongs to the same tree as $i$ since it is this current that has to run through $R_k$ and $L_k$. The term

$$sM_k \sum_{l,m} C_{lm}s(V_l(s) - V_m(s))$$

(A.4)

represents the voltage drop between the primary input and node $i$ due to the current flowing out of node $l$ causing a voltage drop between the primary input and node $i$ due to the mutual inductance $M_k$. The voltage drop at node $a$ due to inductive coupling between two branches $a$ and $b$ is given by $M_{ab}\dot{i}_b$ where $\dot{i}_b$ is the rate of change of the current passing through branch $b$. Hence, voltage drops can occur at node $i$ due to the current at nodes that are not in the same tree as $i$ due to inductive coupling as described by (A.4).

By expanding the voltages in (A.1) into powers of $s$ given by

$$\sum_{r,j} C_{rj}s(V_r(s) - V_j(s)) \quad \text{and} \quad \sum_{l,m} C_{lm}s(V_l(s) - V_m(s))$$

(A.2)
and comparing similar powers of $s$ on both sides of (A.1), the following relations result

\[ m_{0,i} = m_{0,\text{inp}} \tag{A.6} \]

\[ m_{i,i} = m_{i,\text{inp}} - \sum_{k} R_{k} \sum_{r,j} C_{rj}(m_{0,r} - m_{0,j}) \]

\[ m_{n,i} = m_{n,\text{inp}} - \sum_{k} R_{k} \sum_{r,j} C_{rj}(m_{n-1,r} - m_{n-1,j}) - \sum_{k} L_{k} \sum_{r,j} C_{rj}(m_{n-2,r} - m_{n-2,j}) - \sum_{k} M_{k} \sum_{l,m} C_{lm}(m_{n-2,l} - m_{n-2,m}) \]

for $n = 2, 3, 4, \ldots$

These relations allow calculating all the moments, recursively in linear time. Note that the moments of the inputs are known since the inputs are given. For example, if the input signal is given by

\[ V_{\text{inp}}(s) = \frac{m_{0,\text{inp}}}{s} + m_{1,\text{inp}}s + m_{2,\text{inp}}s^2 + \ldots \]

\[ V_{\text{inp}}(s) = \frac{m_{0,\text{inp}}}{s} + m_{1,\text{inp}}s + m_{2,\text{inp}}s^2 + \ldots \]

\[ V_{k}(s) = \frac{m_{0,k}}{s} + m_{1,k}s + m_{2,k}s^2 + \ldots \]

\[ \vdots \]

the moments are given by $m_{0,\text{inp}} = 1$, $m_{n,\text{inp}} = T^n$. For a step input, $m_{0,\text{inp}} = 1$, $m_{n,\text{inp}} = 0$. 

Appendix A: Moments Calculation for Inductively and Capacitively Coupled RLC Trees
Appendix B: RLCK Netlist Reduction

The circuit reduction scheme presented in section 2 can be extended easily to include RLC circuits with coupling-inductors (which are represented by the letter $K$). Fig.B.1 shows the general node $i$ of an RLC circuit with coupling-inductors. In Fig.B.1, each admittance has been decomposed into the generalized RLC branch form of Fig.4.2 and coupling-inductors are added to the $RL$ branch.

![Fig.B.1 A general node in RLC circuit with coupling inductors](image)

The $i^{th}$ row of equation (4.1) is now given by:
Appendix B: RLCK Netlist Reduction

\[
Y{}'V_i + sC_i V_i - y_1 \left( V_1 - \sum_{x=1}^{k_1} sM_{k_1,x} I_{k_1,x} \right) - y_2 \left( V_2 - \sum_{x=1}^{k_2} sM_{k_2,x} I_{k_2,x} \right) - \ldots - y_k \left( V_k - \sum_{x=1}^{k_k} sM_{k_k,x} I_{k_k,x} \right) - sC_1 V_1 - sC_2 V_2 - \ldots - sC_k V_k = 0 \tag{B.1}
\]

where \( y_i = \sum_{j=1}^{k} y_j \) and \( C_i = \sum_{j=1}^{k} C_j \).

Unlike equation (4.2), \( y \) here represents the RL branch only and \( c \) represents the capacitive branch of the generalized admittance. Coupling-inductors are represented by \( M_{j,x} \) (\( j=1..k; \ x=1, 2, \ldots, j_a \)) in equation (B.1) and they induce a voltage drop on the RL branch proportional to \( sM_{j,x} I_{j,x} \) where \( I_{j,x} \) is the current passing through an inductor \( L_x \), which is coupled with the inductor \( L_j \). For generalized admittance \( j \), there are \( j_a \) coupling-inductors. In order to eliminate \( V_i \) from the system, we solve for \( V_i \) using (B.1) and obtain (B.2).

\[
V_i = \frac{y_1 \left( V_1 - \sum_{x=1}^{k_1} sM_{k_1,x} I_{k_1,x} \right) + y_2 \left( V_2 - \sum_{x=1}^{k_2} sM_{k_2,x} I_{k_2,x} \right) + \ldots + y_k \left( V_k - \sum_{x=1}^{k_k} sM_{k_k,x} I_{k_k,x} \right) + sC_1 V_1 + sC_2 V_2 + \ldots + sC_k V_k}{Y_i + sC_i} \tag{B.2}
\]

Equation (B.3) describes the row corresponding to the first neighbor of node \( i \) where \( k_1 \) is the number of nodes connected to node 1.

\[
Y{}'V_i + sC_i V_i - y_1 \left( V_1 - \sum_{x=1}^{k_1} sM_{k_1,x} I_{k_1,x} \right) - y_2 \left( V_2 - \sum_{x=1}^{k_2} sM_{k_2,x} I_{k_2,x} \right) - \ldots - y_k \left( V_k - \sum_{x=1}^{k_k} sM_{k_k,x} I_{k_k,x} \right) - sC_1 V_1 - sC_2 V_2 - \ldots - sC_k V_k = 0 \tag{B.3}
\]

To eliminate node \( i \), we substitute value of \( V_i \) as from (B.2) in equation (B.3) and obtain:
Appendix B: RLCK Netlist Reduction

\[
\begin{align*}
\left( \tilde{Y}_i + s\tilde{C}_i + y_i + sC_i - \frac{(y_i + sC_i)^2}{Y_i + sC_i} \right) y_i - \sum_{s=1}^{k} \frac{y_i + sC_i}{Y_i + sC_i} \sum_{s=1}^{k} W_{rs} - Y_i + sC_i \\
\sum_{r=1}^{k} \left( y_i - \sum_{s=1}^{k} W_{rs} \right) - \sum_{s=1}^{k} sC_i V_r = 0
\end{align*}
\] (B.4)

where \( \tilde{Y}_i = \sum_{r=1, r \neq i}^{k} y_r \) and \( \tilde{C}_i = \sum_{r=1, r \neq i}^{k} c_r \).

where \( \tilde{Y}_i \) is the sum of all admittances (RL) from node 1 except to node \( i \) and \( \tilde{C}_i \) is the sum of all capacitances from node 1 except to node \( i \). Equation (B.4) can be simplified to:

\[
\begin{align*}
\left( \tilde{Y}_i + s\tilde{C}_i + \sum_{j=1}^{k} y_j + sC_i \right) y_i - \sum_{j=1}^{k} \frac{y_j + sC_j}{Y_j + sC_j} \sum_{j=1}^{k} W_{ij} - Y_i + sC_i \\
\sum_{r=1}^{k} \left( y_r - \sum_{s=1}^{k} W_{rs} \right) - \sum_{s=1}^{k} sC_s V_r = 0
\end{align*}
\] (B.5)

Note that this is equivalent to adding \( k-1 \) new elements between node 1 and the \( k-1 \) former neighbors of node \( i \). Equation (B.5) is very similar to equation (4.5) except that the admittances are split between the RL and the C branch and there are additional terms representing coupling-inductors. Specifically, for any two neighbors of node \( i \), say \( m \) and \( n \), the elimination of node \( i \) results in the addition of a new generalized admittance between nodes \( m \) and \( n \) whose equivalence is given by:
Appendix B: *RLCK* Netlist Reduction

\[
(y_m + sc_m)(y_n + sc_n) - (y_n + sc_n)y_m \sum_{x=1}^{m} sM_{m,x} I_{m,x} \\
(y_m + sc_m + y_m \sum_{x=1}^{m} sM_{mn,x} I_{mn,x}) + (y_m + sc_m)y_n \sum_{x=1}^{n} sM_{n,x} I_{n,x} = \frac{Y_I + sC_I}{Y_I + sC_I}
\]

(B.6)

where it is assumed that current flows from \( m \) to \( i \) and from \( n \) to \( i \) before eliminating node \( i \), and it flows from \( m \) to \( n \) after eliminating node \( i \). For low frequency approximation, \( s^2 \) terms in (B.6) are ignored. Thus, when node \( i \) is eliminated, the coupling-inductors present on the \( RL \) branch between node \( m \) and node \( i \) are copied over to the new \( RL \) branch between nodes \( m \) and \( n \). Similarly, all the coupling-inductors present on the \( RL \) branch between node \( i \) and node \( n \) are also copied over to the new \( RL \) branch between nodes \( m \) and \( n \). The inductance, resistance, and capacitance of the new admittance between nodes \( m \) and \( n \) are obtained the same way as for circuits without coupling-inductors. Thus, for circuits without coupling inductors, the elimination procedure falls back to the scheme presented in section 2. Fig.B.2 shows the rules for eliminating node \( i \) for a general \( RLC \) circuit with coupling-inductors. Again, this type of nodal elimination preserves nodal voltages and equivalent branch admittance between nodes, including coupling-inductors. Although the branch currents are not preserved explicitly, they are preserved implicitly because they only depend on nodal voltages and equivalent branch admittances, which are preserved.
Fig. B.2 Rules for eliminating node $i$ in RLCK circuit

Notes:
1. Arrows on inductors indicate assumed current flow direction.
2. For RC, LC, and C branches, rules are same as those in Figure 3.
Appendix C: Patents and Publications of the Author

Pending Patent:


Accepted Journal Papers:


Submitted Journal Papers:


Published and Accepted Conference Papers:


**Submitted Conference Paper:**


Curriculum Vitae

The author was born in Chittagong, Bangladesh on January 14, 1973. After receiving Bachelor of Science degree in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology (BUET), Dhaka in December 1998, he joined as a lecturer in The Department of Computer and Communication Engineering at International Islamic University Chittagong, Bangladesh in January 1999. He has been admitted to the Department of Electrical and Computer Engineering at Northwestern University, Evanston, IL 60208, USA as a graduate student in Fall 2000. After completing necessary course work he passed the qualifying exam to get admitted into the direct PhD program. He was with IBM Austin Research Laboratory, Texas, USA as a summer intern. He is currently working towards his PhD degree in the area of high performance issues in Very Large Scale Integrated (VLSI) CMOS digital circuits. His primary research interests include noise and signal integrity, interconnect issues, inductive effects, innovative circuit analysis technique, and related scaling issues of CMOS VLSI technologies.