ECE 465 — Digital Systems

Fall 2009, T/Th 3:30-4:45 pm, 210 LH

Teaching Staff

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Course Material

Text: *Digital Logic Circuit Analysis and Design*, by Victor P. Nelson, H. Troy Nagle, Bill D. Carroll, David Irwin, Prentice Hall, 1995 (ISBN-10: 0134638948; ISBN-13: 978-0134638942).

Lecture Notes: Almost all will be put online on the course web page:
www.ece.uic.edu/˜dutt/courses/ece465/ece465.html

Homeworks, Projects and Quizes

Homework: Five to six homeworks (HWs) will be assigned. Homeworks are to be submitted ONLY in class on the due date. Late HWs will not be accepted.

Projects: There will be 2-3 projects using the Quartus software. Projects are to be submitted as electronic copies of three main items (some other items may be requested based on the project): (a) the project report, (b) the design or code, as the case may be, and (c) the simulation results, by midnight on the due date. **All** items are to be e-mailed to the TA, and **only** the project report is to be e-mailed to me.

Quizes: There will be 1-2 quizes that will mainly be given to test your preparation of background material that are extremely important for understanding the course material. You will be told about the background material needed for the course material from time to time (a list is also given later in this syllabus) and will be informed of the corresponding quiz.

Examination Schedule

All exams will be closed everything (books, notes, etc.). No make-up exams will be given except in extreme circumstances like a serious health issue that is documented and verifiable. You must contact the instructor prior to the exam in order to arrange for a make-up.

Midterm Exam: In the 8'th or 9'th week of the semseter.
Final Exam: During finals week as scheduled by the official system.

Grade Distribution–approximate

Homeworks	10-15%
Quizes	5-10%
Projects	20-25%
Midterm Exam	20-25%
Final Exam	35%

Honor Code

The following Honor Code policy shall be in effect in this course:

- Not to seek unfair advantage over other students, including, but not limited to: (a) giving or receiving unauthorized aid (i.e., outside of your official project work team) during completion of academic requirements (this includes lab work, homeworks and exams); (b) obtaining past semseters' project and homework solutions and creating your project/homework from them.

  For your information, we have electronic copies of past student projects and can verify if your project's design/code has any similarity with that of past projects (even if you change entity names and or some parts of a past project). Past students have also been told not to give anyone their projects or homework solutions, and to report if anyone asks for them. So, please do not even think of asking for these, if you value honesty, fairness, and your status as a student in good standing at UIC.

- To represent fact and self truthfully at all times.

- Not to pass on your project work or homework solutions to anyone else ever, either in this semseter, or at any future time including after you graduate.

Violations of the Honor Code are just causes for discipline under the University of Illinois at Chicago Student Disciplinary Procedure, and all allegations of Honor Code violations shall be handled pursuant to that Procedure.

Course Outline

Note: The sections of the text listed below in square brackets for the various topics may not always cover all subtopics discussed in class or may cover more subtopics than discussed in class, as the book will not be followed 100%. Handouts will be given on some ocassions. But mainly it is important to attend all lectures in order to learn all the material and do well in the course. Lecture #s for each topic corresponds to 1 hr 15 min lectures.

1. **Introduction (1.5 lecture)** (Sec. 0.2).

2. **Review of Basics (1.5 lectures)**
   Boolean algebra, fundamental definitions (implicants, prime implicants, implicates, prime implicates, etc.), minimization using Boolean algebra, minimization using K-maps, hazards in combinational circuits and their solutions, synthesis using NAND/NOR gates [1.1, 1.3-1.4, 2.1-2.2, 2.5, 3.1-3.8]

3. **Advanced Two-level Combinational Circuit Minimization (4 lectures)**
   Quine-McCluskey method (single and multiple functions), Petrick's algorithm [3.9-3.10]

4. **Component-Based Combinational Circuit Synthesis (MUXes, PLAs, PALs) (4 lectures)** [4.2, 4.4, 5.1-5.5]

5. **High-Level Design Approaches including Divide-&-Conquer (3 lectures)**

6. **Synchronous Sequential Circuits (9 lectures)**
   finite state machine (FSM) synthesis (Moore, Mealy), synthesis of synchronous sequential circuits, clocking methods, state minimization and state assignment techniques, one-hot design style [8.1-8.4, 9.1-9.4]

7. Either:
   (a) Testing of Combinational and Sequential Circuits (4 lectures) [12.1-12.4]

   Or
   (b) Asynchronous Sequential Circuits (4 lectures)
   Synthesis (pulse & fundamental modes), races and hazards [10.1-10.6]

Background Review Material

Please diligently review the following background material for ECE 265 for you to understand the lectures in ECE 465 and do well in the quizes. The secs. in text where these material are available are listed in square brackets. The week # given is the week in which these meterial have to be reviewed by you.

1. **Introduction:** [0.1-0.2] – week 1
2. **Number Systems and Codes:** [1.1-1.2] – week 1
3. **Boolean Algebra:** [2.1-2.2] – week 1
4. **K-maps:** [3.1-3.7] – weeks 1 and 2
5. **Logic gates, synthesis of logic circuits using NAND/NOR gates:** [2.3-2.4.1, 2.5-2.6] – week 2
6. **Latches and FFs:** [6.1-6.4.2 except the discussion on 74LS75 and 74116 D-latches] – week 7