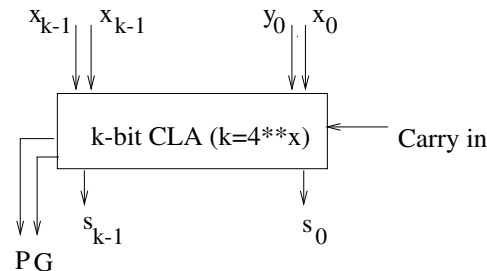


ECE 465, Spring 2005, Instructor: Prof. Shantanu Dutt

Homework 3 : Due Tue, April 19

1. You have the following components: 1) Two 16-bit tree carry-look ahead adders (CLAs); 2) One 4-bit CLA. Using these components you need to design a 36-bit tree CLA. Each of the above components have composite P, G signals available; a generic k -bit tree CLA component is shown below.



A k -bit CLA component

(a) Derive the SOP logic expressions that generate the carry inputs to two of the above components (the carry in to one of the components will be C_{in} , which is the carry in to the entire adder) as well as C_{out} . **100**

(b) Show the block diagram of your 36-bit tree CLA with the above carry generation unit and the three CLA units as components. Show all interconnections between these components (show each component as a rectangular box with appropriate inputs and outputs; don't show its internal gate interconnections), C_{in} and C_{out} . **50.**

(c) Derive the worst-case delay of your 36-bit tree CLA assuming that the delay of any AND/OR/NOT/XOR/XNOR/NAND/NOR gate with k inputs is k .

You can use the delay expressions for P, G generation and for carry generation of a 4^x -bit tree CLA for $x \geq 1$ that was done in class (see Lecture Notes on "Fast Adders"). However, please state these expressions correctly and explicitly before using them in the delay calculation of the 36-bit tree CLA. **150**

2. Prob. 8.13 (do Mealy for (a) & (d) and Moore for (b) & (c)). Label the states so that it is clear what they represent; just drawing circles and arrows is not enough. Note that by the labeling of a state we mean a symbolic description of the state's function and/or what it remembers about past inputs (e.g. "Even" state in the parity checker [Lecture Notes on "Sequential Circuit Synthesis"] corresponds to the state which remembers that the number of 1's so far is an even number). Also note that by labeling we **do not** mean the encoding of a state in binary bit values (that is called "state assignment"). **120**
3. Prob. 8.25 (note that a counter is just an FSM with no extra external outputs beyond the state bits—the state bits also serve as the counter output). **80**
4. Obtain a state-transition diagram for a Mealy FSM for a vending machine controller with the following specifications: It dispenses gum for 15 cents and accepts nickels, dimes and quarters inserted one at

a time. Three sensors detect which type of coin has been inserted and a 4-to-2 encoder converts the 3 outputs of the sensor into a 2-bit input x_1, x_2 to the FSM ($x_1x_2 = 00$ means no coins inserted, $= 01$ means a nickel inserted, $= 10$ means a dime inserted, and $= 11$ means a quarter inserted). It returns change; assume that the user will not put in more than a total of 25 cents and that the amount of change to be returned is always available. Three outputs are required from the FSM, one is "OPEN" for dispensing gum and the other two y_1, y_2 for controlling coin return ($= 00$ for no change, $= 01$ for 5 cents change, $= 10$ for 10 cents change).

Draw a clear block diagram of the system (see, e.g., the block diagram of the simpler vending machine system in the lecture notes on "Sequential Circuit Synthesis") and then give the FSM's state-transition diagram. Label the states so that it is clear what they represent. **100**