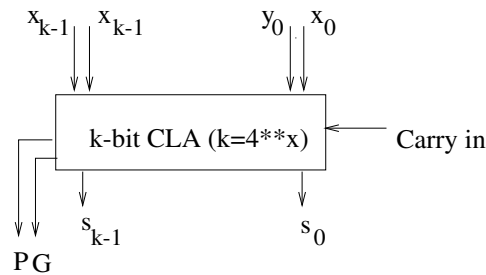


## ECE 465, Instructor: Prof. Shantanu Dutt

### Solution to 32-bit CL – Homework 3

Problem 1: Design and Analysis of a 36-bit Tree CLA

You have the following components: 1) Two 16-bit carry-look ahead adders (CLAs); 2) One 4-bit CLA. Using these components you need to design a 36-bit CLA. Each of the above components have composite  $P, G$  signals available; a generic  $k$ -bit CLA component is shown below.



*A k-bit CLA component*

(a) Derive the SOP logic expressions that generate the carry inputs to two of the above components (the carry in to one of the components will be  $C_{in}$ , which is the carry in to the entire adder) as well as  $C_{out}$ . **15**  
Ans: We will denote the different *propagate* and *generate* signals in a CLA as follows.  $p_i, g_i$  for the propagate and generate produced by the  $i$ 'th modified full adder. These are single-bit propagate and generate signals. Subsequently, each group composed of up to four of the previous level CLAs generate their composite propagate and generate signals  $P_{j,x}, G_{j,x}$ , where  $j + 1$  is the *level* of the next larger group, defined as  $j + 1 = \lceil \log_4(k) \rceil$ , where  $k$  is the number of input bits being handled by the next larger group (of up to 4 current level groups).  $x$  the second index is the position of a current-level group counting left to right and ranging from 0 to up to 3. See the figure below for examples of this notation.

According to the above notation and as shown in the figure below, the  $P, G$  inputs to the carry generation unit (CGU) are  $P_{2,0}, G_{2,0}, P_{2,1}, G_{2,1}$  and  $P_{2,2}, G_{2,2}$ . Note that since the number of bits is 36 (and not 64 the next higher power of 4 after 16), this CGU is “truncated” in that its inputs are 3 pairs of  $P, G$ 's (instead of the normal 4 pairs) and it has 3 carry outputs (instead of the normal 4). The carry equations are:

$$C_{16} = G_{2,0} + P_{2,0} \cdot C_{in}$$

– delay of  $C_{16}$  (from its inputs) = 4 units

$$C_{32} = G_{2,1} + G_{2,0} \cdot P_{2,1} + P_{2,1} \cdot P_{2,0} \cdot C_{in}$$

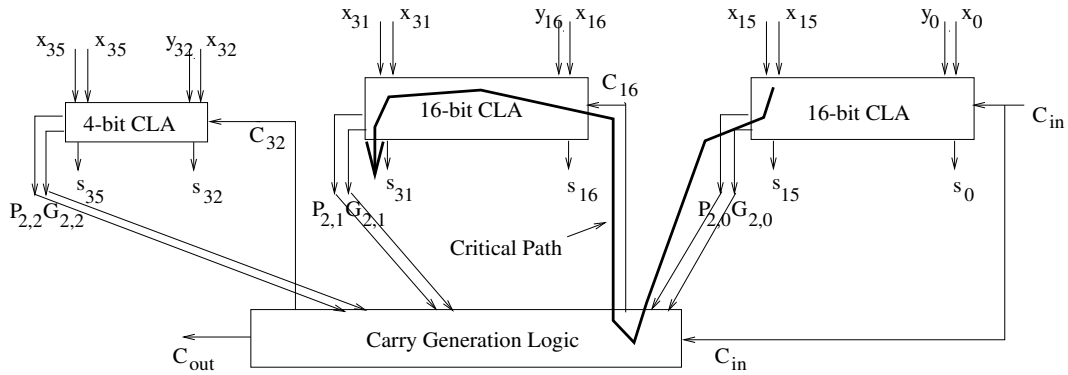
– delay of  $C_{32} = 6$  units

$$C_{out} = G_{2,2} + G_{2,1} \cdot P_{2,2} + G_{2,0} \cdot P_{2,2} \cdot P_{2,1} + P_{2,2} \cdot P_{2,1} \cdot P_{2,0} \cdot C_{in}$$

– delay of  $C_{out} = 8$  units

(b) Using this carry generation unit, show all interconnections between it (show it as a rectangular box with appropriate inputs and outputs; don't show the internal gate interconnections),  $C_{in}$ ,  $C_{out}$  and the 3 CLA units. **15.**

Ans:



*Schematic of a 36-bit CLA*

(c) Derive the worst-case delay of your 36-bit adder assuming that the delay of any gate with  $m$  inputs is  $m$  units.

If you want, you can use the delay expressions for  $P, G$  generation and for carry generation of a  $4^x$ -bit CLA for  $x \geq 1$  that was done in class. However, please state these expressions correctly and explicitly before using them in the delay calculation of the 36-bit CLA. **25**

Ans:

To refresh, the general  $P, G$  generation logic for level  $j$  using the 4 previous level's four  $P, G$  signals is:

$$P_{j,x} = P_{j-1,3} \cdot P_{j-1,2} \cdot P_{j-1,1} \cdot P_{j-1,0}$$

$$G_{j,x} = G_{j-1,3} + G_{j-1,2} \cdot P_{j-1,3} + G_{j-1,1} \cdot P_{j-1,3} \cdot P_{j-1,2} + G_{j-1,0} \cdot P_{j-1,3} \cdot P_{j-1,2} \cdot P_{j-1,1}$$

– delay of composite  $P_{j,x}, G_{j,x} = 8$  units.

Also, the general carry signal generation logic by a regular CGU with 4 input pairs of  $P, G$  signals and 4 output carries  $C_1, C_2, C_3, C_4$  is:

$$C_1 = G_{j,0} + P_{j,0} \cdot C_{in}$$

$$C_2 = G_{j,1} + G_{j,0} \cdot P_{j,1} + P_{j,1} \cdot P_{j,0} \cdot C_{in}$$

$$C_3 = G_{j,2} + G_{j,1} \cdot P_{j,2} + G_{j,0} \cdot P_{j,2} \cdot P_{j,1} + P_{j,2} \cdot P_{j,1} \cdot P_{j,0} \cdot C_{in}$$

– delay of  $C_3$  (from its inputs) = 8 units.

$$C_4 = G_{j,3} + G_{j,2} \cdot P_{j,3} + G_{j,1} \cdot P_{j,3} \cdot P_{j,2} + G_{j,0} \cdot P_{j,3} \cdot P_{j,2} \cdot P_{j,1} + P_{j,3} \cdot P_{j,2} \cdot P_{j,1} \cdot P_{j,0} \cdot C_{in}$$

– delay of  $C_4$  (from its inputs) = 10 units.

Of the above carry delays,  $C_3$  is the most crucial as it inputs to a previous-level CLA as its  $C_{in}$  input and is used to generate carry's to even more previous levels of CLAs until carries are generated as inputs to each modified full adder.  $C_4$  is only used as the  $C_{out}$  of the entire adder from the highest level CGU and is not utilized for lower-level CGUs. So the critical path will not go through it.

Furthermore, a little thought leads to determining the critical path as going via the highest level  $P, G$  generation logic and then  $C_{16}$  into the two levels of CGUs of the second 16-bit CLA to generate  $C_{31}$  followed by the generation of  $S_{31}$ . This is shown by a dark path traced through the schematic of the 36-bit CLA shown above. The critical path will not go via  $C_{32}$  to the 4-bit CLA and finally to  $C_{35}$  and then  $S_{35}$ , as even though  $C_{32}$  takes 2 units more time to be generated than  $C_{16}$ , it encounters only one level of CGU

to generate  $C_{35}$ —each CGU's relevant delay is 8 units, thus the path to  $S_{31}$  will take  $8 - 2 = 6$  units more time than the path to  $S_{35}$ .

The delay of the above critical path has the following generation delays:  $p_i, g_i$  generation (2) + two levels of  $P, G$  generation in the 1st 16-bit CLA ( $8 + 8 = 16$ ) + generation of  $C_{16}$  at the highest level CGU (4) + two levels of carry generation via 2 levels of CGUs in the 2nd 16-bit CLA [in particular the third carry generated in each CGU is in the critical path] ( $8 + 8 = 16$ ) + generation of  $S_{31}$  [after  $C_{31}$  is generated] (2)

$$= 2 + 16 + 4 + 16 + 2 = 40 \text{ units.}$$