

ECE 465, Fall 2009, Instructor: Prof. Shantanu Dutt

Homework 4 : Due Tue, Nov. 3

1. Prob. 5.2(b) and (d) from the text. For 5.2(d) use the PAL schematic given in Fig. 5.28 and not Fig. 5.30.

For the PLA design, use the multi-function QM method using a PI cost of 1 to share as many product terms as possible between the three functions, thereby minimizing the cost of the implementation.

For the two problems, specify the PLA/PAL size in terms of inputs, outputs and product lines needed for the three functions. **100**

2. (a) Design a 3-bit ripple-carry adder using an appropriate PLA with feedback (using a schematic of the type shown in Fig. 5.14). Specify the PLA size in terms of inputs, total outputs, outputs that feedback to the AND-plane of the PLA, and product lines needed for the design. Obtain the design **without** using multi-function QM. **50**

(b) Give clearly stated rationale on whether it is beneficial or not to use multi-function QM for this particular design (Hint: Think of how much product term sharing is possible). **30**

3. Use the divide-and-conquer (D&C) approach to design a combinational multi-bit left-shifting circuit MUBILS with inputs an n -bit number X (the shiftee) and a $\log_2 n$ bit # m (the shift amount) and outputs a $(2n-1)$ -bit number Z that is X shifted m times. E.g., if $X = 11000111$, and $m = 110 = 6$, then X needs to be shifted by 6 bits and $Z = 011000111000000$.

Show the general (for an n -bit X) D&C breakup of this problem and actually solve the problem for $n = 16$, clearly showing the basic design for shifting X by a 1-bit number (this will be the smallest subproblem at the leaf of your D&C tree) and how two smaller designs are “stitched up” to provide the next larger design, and so forth. **Show all your work in clear and methodical steps.** **200**

Hint: Perform the D&C of the design on the shift amount m , i.e., the problem is broken up into shifting X by a certain number of bits based on a single bit of m followed by shifting the result based on the rest of the bits of m . The latter computation is further broken down in a similar D&C manner.