

ECE 465, Fall 2009, Instructor: Prof. Shantanu Dutt

Homework 3 : Due Thurs, Oct. 22

1. Prob. 3.63 using the alternate to Rule 6 followed by the sweep-up phase. **80**

2. Redo the PIT (covering) part of the 3-function multi-function QM done in class (and given in the notes) using Rule 6 (the example given in the notes does not use Rule 6). **60**

3. Determine the number of transistors needed for designing a 64:1 MUX using the following approaches:
 - (a) The “flat” approach using a generalized truth table and logic gates. For this assume that you can use up to 5-input gates, each input corresponds to 2 transistors in a gate, and that select inputs and their complemented forms are available (i.e., you do not need NOT gates to generate them). **20**
 Obtain a general expression for the number of transistors in a $2^n : 1$ MUX using this approach. **20**
 Is there any drawback to using T-gates in this approach for large MUXes (such as 64:1 MUX)? Explain what the problem is, and how it can be fixed. **30**

 - (b) A divide-and-conquer (D&C) approach in which T-gates are used to construct the basic 2:1 MUXes. Here also assume that select inputs and their complemented forms are available. **20**
 Obtain a general expression for the number of transistors in a $2^n : 1$ MUX using this approach. **20**

4. Implement a 2-bit adder function (i.e., a 2-bit binary number a_1a_0 added to another 2-bit binary number b_1b_0 to yield a 3-bit sum $s_2s_1s_0$) using three 8:1 MUXes. Derive the TT and show all steps clearly for deriving the (data) inputs to the MUXes. **40**

5. Implement the function $f(A, B, C, D) = \sum m(2, 4, 5, 8, 10, 12, 13, 14)$ using a 4:1 MUX and a choice of 2 control variables such that a minimal number of 2-i/p AND/OR gates are used. Assume that the inverted inputs of all variables are available for free. **50**