ECE 465, Fall 2009, Instructor: Prof. Shantanu Dutt

Homework 1 : Due Thurs, Sept. 23

1. Prove that the single parity code method for a set of n information bits $x_{n-1}, x_{n-2}, \ldots, x_0$ can detect any number of odd errors in the informaton bits and the check bit x_c. Recall that the check bit is determined as:

   $$x_c = x_{n-1} \oplus x_{n-2} \oplus \ldots \oplus x_0.$$

   Note also that the method used for detecting if there is an error in the received bits $\hat{x_{n-1}}, \ldots, \hat{x_0}, \hat{x_c}$ is to check if the following equality holds:

   $$\hat{x_c} = \hat{x_{n-1}} \oplus \hat{x_{n-2}} \oplus \ldots \oplus \hat{x_0}.$$

   If the equality holds, then there is no error (with high probability), otherwise an error is detected.

   You can use an approach similar to the one used in class to prove that this parity scheme will not detect errors that are even in number. You can also use tha fact that the number of 1's in the correct information plus check bits is even. **75**

2. Prove that for two implicants g and h of a function f to be *adjacent* (two implicants are adjacent if their product terms are the same in all variables except one, which occurs in complemeneted form in one implicant and in uncomplemented form in the other), the number of 1's in their ternary notations need to differ by exactly one. (Note that, as the statement asserts, this condition is *necessary* but not *sufficient* for g and h to be adjacent). **75**

3. Prove that in QM's tabular method for forming PIs, if an implicant g cannot be combined with (i.e., is not adjacent to) any other implicant in its column, then it is a PI.
   Hint: Use the fact that any implicant covers or contains 2^i minterms, where $i \geq 0$. **75**

4. (a) Determine a minimized SOP expression for the $\log_2$ function f of a 4-bit number N. Specifically, this function gives the rounded-up integer value (i.e., the *ceiling*) of $\log_2 N$. Thus, e.g., $f(7) = 3$, $f(8) = 3$, $f(9) = 4$, $f(15) = 4$. The minimized expression for each output bit can be obtained using either the K-map or the QM technique. **75**

   (b) Implement and simulate your gate-based design obtained above using the Quartus II CAD software as specified below. **150**

   - Choose the schematic capture tool in Quartus to specify your design.
   - Perform simulations based upon the input file provided by the TA.
   - Device family to be used for the project is Cyclone which is selected by default in Quartus.
   - Report: (i) the logic/hradware cost of the Quartus implementation in terms of the total # of gate inputs, and (ii) the circuit delay obtained by Quartus simulation—this is the maximum of all delays you obtain by simulating the different inputs provided to you.
   - Submit the printed Quartus schematic of the design.
   - Submit the design file to the TA by email.
   - Submit the simulation output file to the TA by email.