

ECE 465, Spring 03, Instructor: Shantanu Dutt

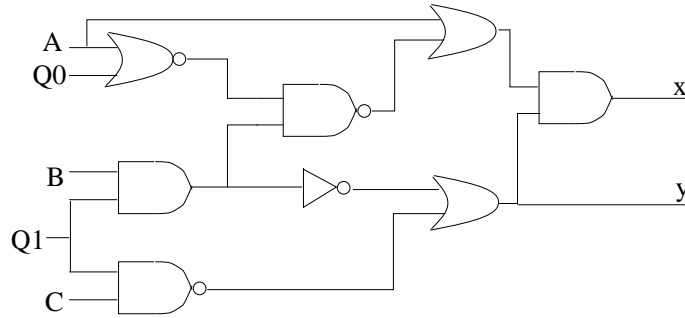
Final Exam : Thurs, May 8, Time: 3:30 to 5:30 PM

Exam Format: Closed Book, Total Points: 180

Important Note: You need to show all your work clearly in deriving the answers. Just writing down the final answers is not enough.

Suggestion: Begin by reading all questions and do those first that you think you know best.

1. **Timing Methodology:** There is a **2-phase** clocked sequential circuit for which the combinational logic is given below (for simplicity, we assume that the circuit has no external outputs). The max delay of a gate is given by the expression $3m$ nsecs (ns) and the min delay of a gate is given by the expression $2m$ ns, where m is the number of inputs to the gate. Note that inverters (NOT gates) have $m = 1$. Assume that for the external inputs, complemented inputs are also available, and note also that for a FF both Q and \bar{Q} are available. The delay data for a D-FF is as follows: $T_{su} = 20ns$, $T_h = 5ns$, typical $T_{plh} = 25ns$, $\min T_{plh} = 13ns$, typical $T_{phl} = 40ns$, $\min T_{phl} = 25ns$. Finally, assume that the system clock skew is 7 ns.



Next-State Logic: External I/Ps: A,B,C; Current state bits: Q0, Q1;
Master FF excitation inputs: x, y

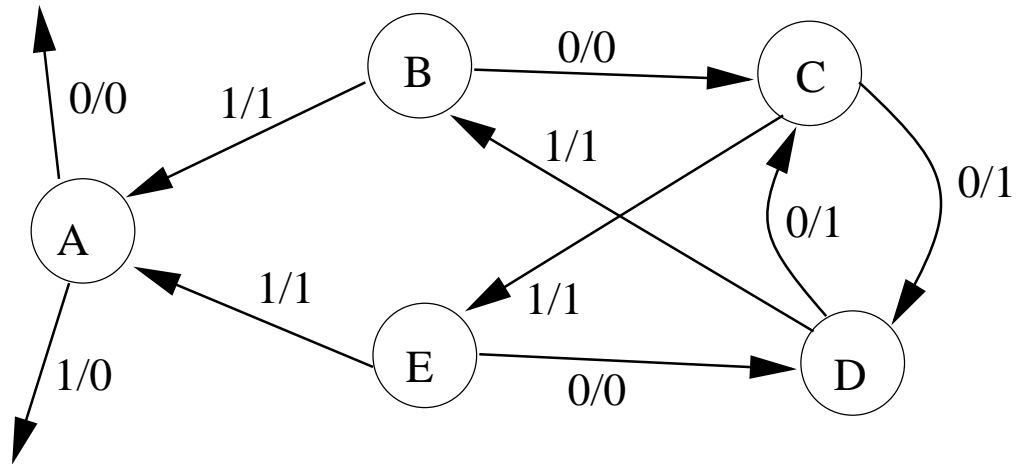
(a) Assuming that the combinational logic is in one block between the slave and master FFs (i.e., the traditional or classical configuration), determine the clock period. Note that the clock period should have a 10% safety margin (i.e., be 10% greater than the minimum that it can be.) Show your work clearly. **20**

(b) In order to reduce the clock period, split the combinational logic into two parts so that the max path delays in the two parts are roughly equal. Place the 1st part after the slave FFs (i.e., inputs to the first part are the external inputs A, B, C and state bits Q_0, Q_1). Each output of the first part (these outputs correspond to the wires that are “cut” by the split you perform) is an input to a unique “master” D-FF, and each output of a master D-FF is an input to the 2nd part of the combinational logic. Finally, the outputs of the 2nd part are inputs x, y to the two slave D-FFs that store the state bits (Q_0, Q_1) .

Clearly draw the complete sequential circuit (along with all required D-FFs) resulting from the above split you perform for the given combinational logic.

Finally, determine the resulting clock period corresponding to the above split of the combinational logic. Once again, note that the clock period should have a 10% safety margin. Show all your work clearly. **50**

2. **State Minimization:** A portion of an FSM is shown below.



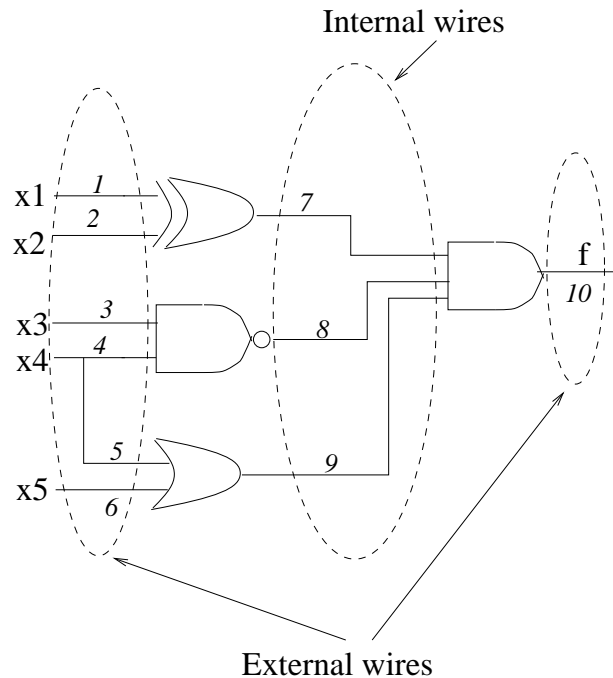
Determine from 1st principles (i.e., using the basic definition of equivalency of two states) which pairs of states shown are equivalent and **prove** these equivalencies for each equivalent pair also from 1st principles. Note that such proofs were discussed in class (for e.g., that two states X, Y are equivalent if their implied next state pairs are a combination of singleton states and the same state pair (X, Y)), and you can use the same proof approach. **50.**

3. **Testing:** For the circuit shown below (wires are labeled in italics):

(a) Find all test vectors for each fault only on the internal wires (7, 8, 9) using the **path-sensitizing method**. Note that there will be a total of six faults, two on each internal wire.

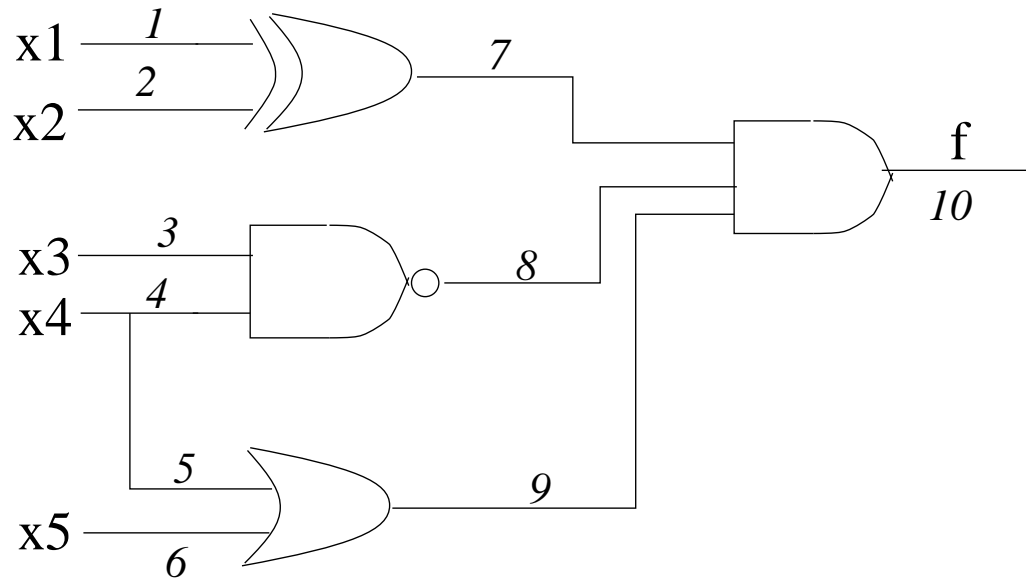
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(b) Construct a **fault table** for only the internal wires (7, 8, 9) of the circuit and, as done in class, determine a **minimal test set** for only these internal wires from this table using techniques similar to that used for a PIT to choose a minimum set of PIs to cover all the minterms. (Here the tests are similar to PIs, the faults are similar to minterms and the cost of each test is 1). Note that the rows of the fault table should only be the test vectors for the six internal faults and should not be all the 2^5 combinations of the 5 inputs. Show all steps clearly. **20**

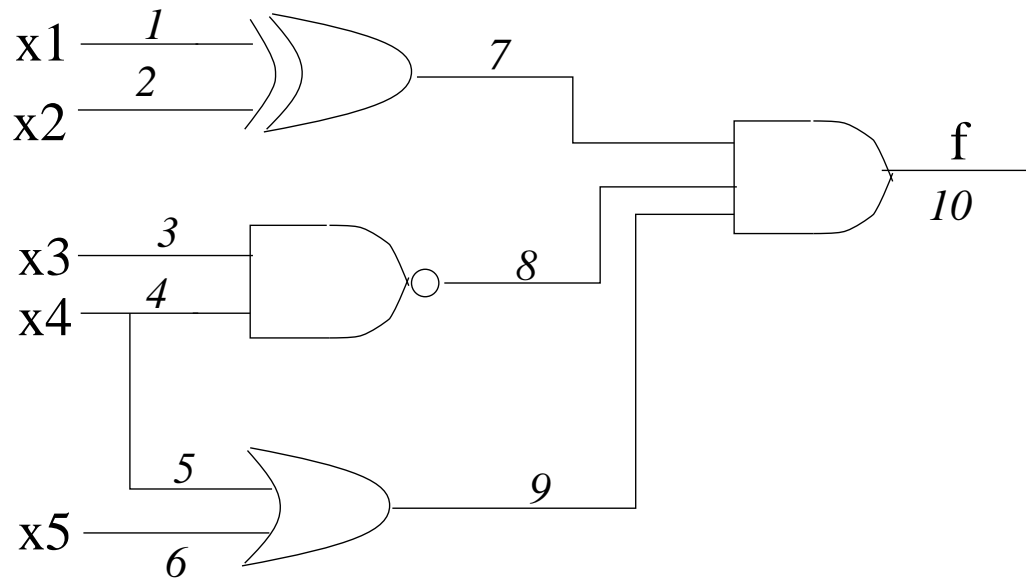


For your convenience, 6 copies of the circuit are given in the following 3 pages. You need to derive the tests for each internal wire fault on each of the given copies of the circuits (use one copy for each fault) as indicated above each figure. **Write your name on the Q sheet front page and submit it along with your answer sheet.**

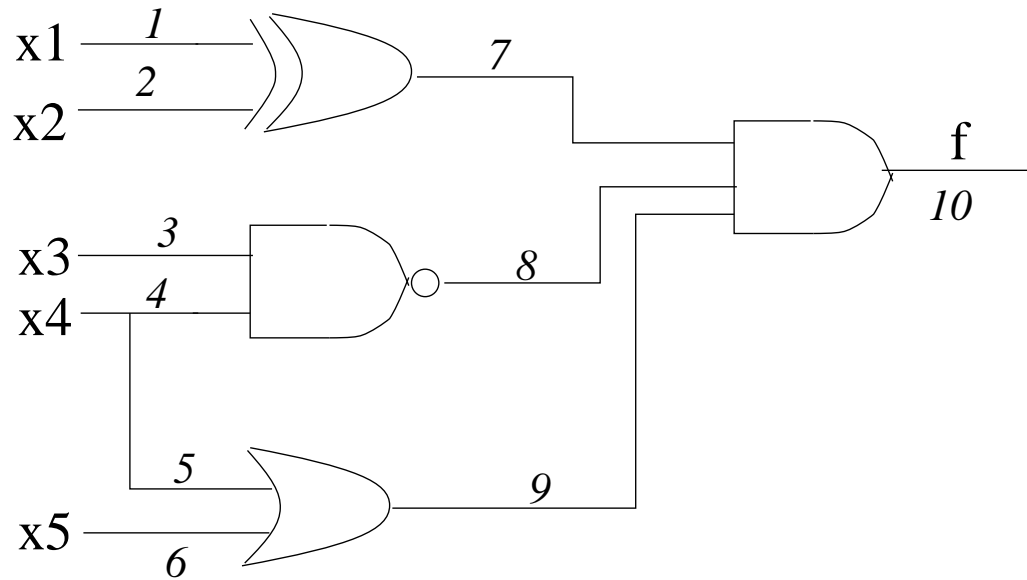
(i) For fault 7/0:



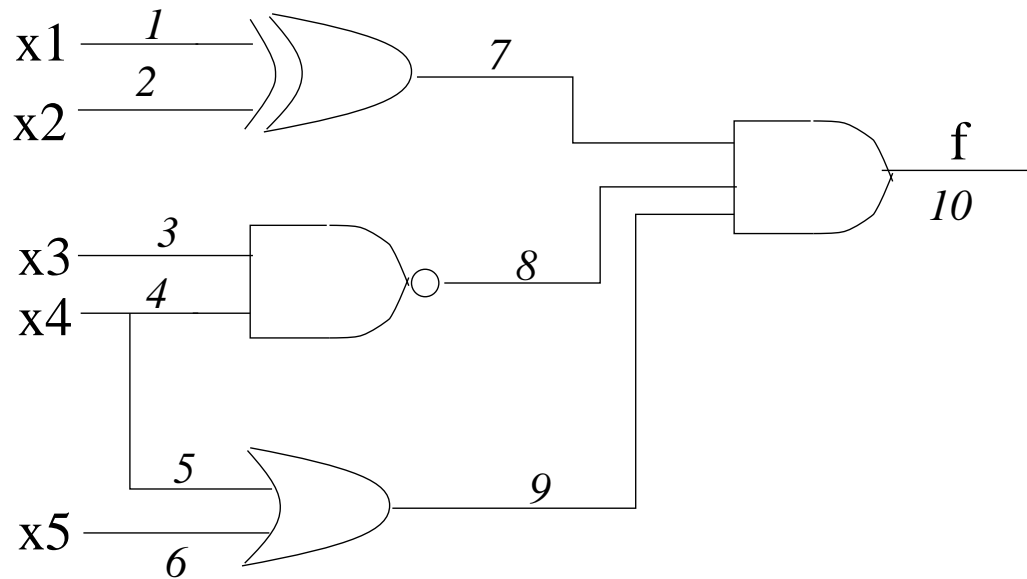
(ii) For fault 7/1:



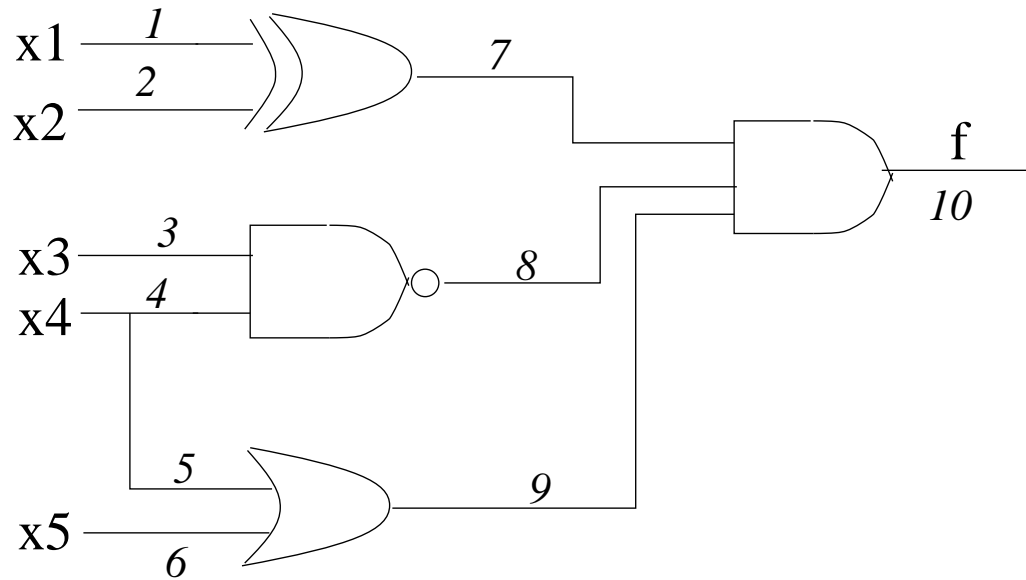
(iii) For fault 8/0:



(iv) For fault 8/1:



(v) For fault 9/0:



(vi) For fault 9/1:

