

ECE 368 — CAD Based Logic Design

Spring 2009
MWF 3-3:50 pm, 316 DH

Teaching Staff

Instructor: Professor Shantanu Dutt, 355-1314, 930 SEO
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Instructor's Office Hours: T/Th: 4-5pm, W: 4:30-5:30pm

Course web page: <http://www.ece.uic.edu/~dutt/courses/ece368/ece368.html>

Check this page periodically for important messages and announcements.

Teaching Assistant: TBD

Office Hours: TBA

Course Material

Text: *The Designer's Guide to VHDL*, Peter Ashenden, Morgan Kaufman, 2nd Ed., 2002 (# ISBN-10: 1558606742 # ISBN-13: 978-1558606746)

Reference Text: *Digital Logic Circuit Analysis and Design*, V.P. Nelson, et al., Prentice Hall, 1995.

Lecture Notes: have been posted on the course webpage and will be updated periodically. It is very important for you to print out the lecture notes so that you can follow the class lectures that will mostly use these notes. Most of the class material will be based on these notes which have partly been derived from the text and other VHDL and digital design sources.

Homeworks and Lab Assignments

- About seven combined homework and lab assignments will be given. They will be due in the lab on the date specified. Hardcopy of the lab reports as well as electronic copies of the report and the VHDL code are to be submitted. The electronic copies need to be submitted by email both to the TA and to Prof. Dutt.
- In general, your lab report should contain the following sections (if others are asked for explicitly in a lab, those should be provided as well):
 - Design Solution Your well-explained design solution with figures and other supporting material as appropriate for the design
 - Design Analysis A clearly presented analysis of various metrics of your design including hardware cost, timing/delay, etc., as required for the lab.
 - Simulation Report A clearly presented report of all the simulations performed (as specified for the lab) to ascertain the correct working of your design including the graphic output of the VHDL simulator and any necessary tables to report needed metrics (e.g., circuit timing or delay)
 - Findings and Conclusions Your findings and conclusions from the simulations performed for your design, as required for the lab (e.g., how does it compare to some standard design studied in class, how do metrics obtained by simulation match the expected or theoretically-analyzed metrics)

- Late lab submissions will not be accepted.
- The minimum threshold for getting any points in a lab is that your design **should work correctly** as determined by simulating of your design (to be done and reported by you as part of your lab work and to be checked by the TA during grading). This is necessary as “partial credit” for incorrect or non-working designs does not exist in the real world, and this standard to work ethic needs to be learnt during your education.

Honor Code

The following Honor Code policy shall be in effect in this course:

- Not to seek unfair advantage over other students, including, but not limited to: (a) giving or receiving unauthorized aid (i.e., outside of your official lab work team) during completion of academic requirements (this includes lab work, homeworks and exams); (b) obtaining past semesters’ lab and homework solutions and creating your lab work/homework from them.
- To represent fact and self truthfully at all times.
- Not to pass on your lab work to others who may not be taking ECE 368 this semester (but may take it in future semesters)

Violations of the Honor Code are just causes for discipline under the University of Illinois at Chicago Student Disciplinary Procedure, and all allegations of Honor Code violations shall be handled pursuant to that Procedure.

Examinations

Exams will be generally be open book (text and other VHDL notes for syntax reference). No make-up exams will be given except in extreme circumstances like a serious health issue that is documented and verifiable. You must contact the instructor prior to the exam in order to arrange for a make-up.

Midterm Exam: tentatively end of the 9th week of classes)

Final Exam: During finals week as scheduled by the official system.

Grade Distribution

Homeworks & Labs	50%
Midterm Exam	20%
Final Exam	30%

Course Outline

1. The Art of Digital Design
2. Combinational Circuits and their VHDL Description
3. Arithmetic Circuits
4. Sequential Circuits and their VHDL Description
5. Controller and Datapath Design
6. Advanced VHDL Concepts

Background Review Material

Please review the following background material from ECE 265 for you to understand the lectures in ECE 368. The secs. in the reference text where these material are available are listed in square brackets. The week # given is the week in which these material have to be reviewed by you.

1. Introduction: [0.1-0.2] – week 1
2. Number Systems and Codes: [1.1-1.2] – week 2
3. Boolean Algebra: [2.1-2.2] – week 2
4. Logic gates, synthesis of logic circuits using NAND/NOR gates: [2.3-2.4.1, 2.5-2.6] – week 2
5. Latches and FFs: [6.1-6.4.2 except the discussion on 74LS75 and 74116 D-latches] – week 6
6. Sequential Circuit Synthesis – week 6