

ECE 368—Spring 2009, Instructor: Prof. Shantanu Dutt

Lab 2 : Due Thurs, Feb. 5 (end of lab)

Purpose

(1) Refresh basic logic design and sharing of gates among multiple functions to reduce cost; (2) Structural VHDL description of a multiple-function (i.e., multiple output) circuit using basic gates; (3) Determining (worst-case) circuit delay analytically and determining delay via simulation.

Design Problem

1. Obtain the minimized SOP expression followed by the gate realization of a BCD-to-seven-segment decoder (input is a 4-bit BCD # from 0 to 9 and output is 7 bits a, b, c, d, e, f, g each controlling a segment of a 7-segment display for displaying the input #) using the following type of gates taking care to generate common product terms across two or more functions only once in order to reduce hardware cost:

(a) NOT gates, and AND and OR gates with at most 4 inputs.

To obtain the minimized multifunction SOP expression you can either: (i) use the multi-function Quine-McCluckey minimization method (see Digital Logic Circuit Analysis and Design, V.P. Nelson, et al., Prentice Hall, 1995), or (ii) use the K-map method for each individual function and obtain maximum sharing of product terms among the 7 functions by observation.

200

Define the *cost* of an SOP (POS) expression of a single function to be the total [# of literals across all product (sum) terms that have more than 1 literal] + [the # of product (sum) terms].

The *total cost* of SOP (POS) expressions of multiple functions is defined as [# of literals across all *unique/distinct* product (sum) terms that have more than 1 literal] + [the # of product (sum) terms].

Define a *circuit/hardware cost* as the total # of gate inputs (i.e., total # of inputs across all gates).

(c) What is the total cost of the SOP expressions for the functions for a, b, c, d, e, f, g in your SOP design? **20**

(d) What is the circuit cost for part (a)? **20**

(e) Assume that the delay of a k -input gate is $3k$ ns. Calculate the circuit delay (i.e., the delay of the *critical* or maximum-delay path) for the above circuit design; see the appendix for a delay calculation method. **40**

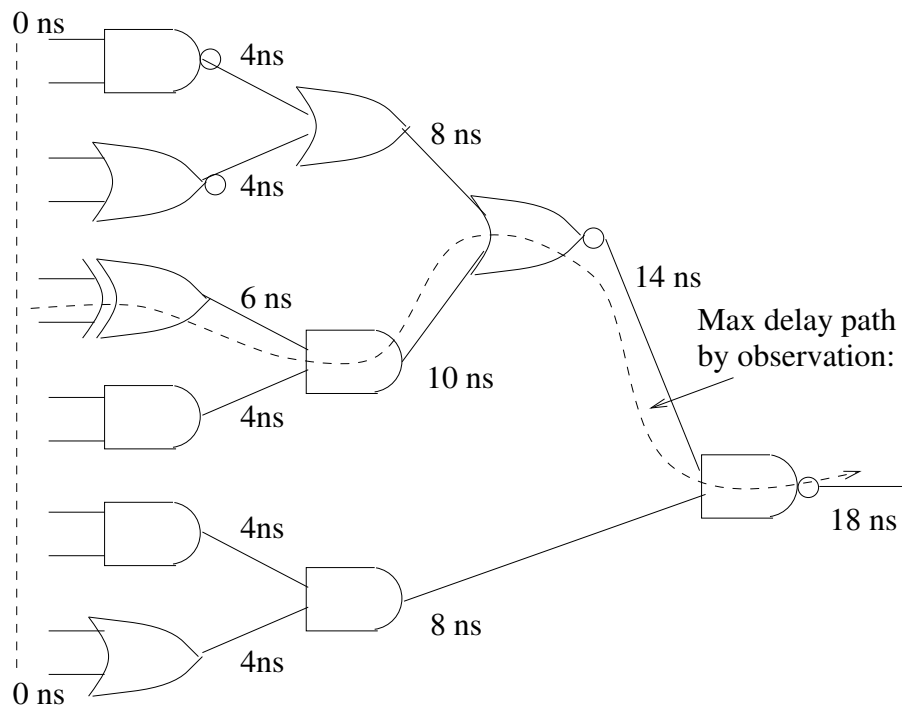
2. Describe your BCD-to-7-segment design in VHDL using the structural model with the components as 2-, 3-, 4-input AND, OR gates and NOT gates (describe these components behaviorally with delays as defined above); once again use sharing of subcircuits/gates among the 7 functions as much as possible to reduce hardware cost. Compute the delay of the design. Also, determine the hardware cost of this description. **100**

Simulation and Testing

Using a testbench with placeholders for your circuit descriptions that will be provided to you: (a) instantiate your VHDL description, and (b) test it by inputting all 10 digits (0-9) to these designs (done by the TB) and determine and tabulate the correctness of the outputs by manually noting the digit that will appear on the 7-segment display at the output based on the values on a, b, c, d, e, f, g displayed by the VHDL simulator.

Also, determine the maximum *simulation delay* obtained for your VHDL description over all the 10 inputs using the VHDL simulator. Discuss how well does this simulation delay correlates with the analytical delay you computed for your circuit description (i.e., the delay of the design of part (b)) and any discrepancies between them. 150

Appendix – Determining circuit delay



Delays: 2-i/p gates, AND, OR, NAND, NOR: 4ns, XOR, XNOR: 6ns

Determining the max. delay of a circuit:

(1) Path tracing by observation -- prone to human error in large circuits

(2) Recursive formulation: Delay at o/p of gate $g_i = \max\{\text{delay of all i/ps to } g_i\} + \text{delay of gate } g_i$

Delay of a circuit = $\max\{\text{delay at all o/ps}\}$