

LAB INSTRUCTION FOR SETTING UP THE SYNOPSIS VHDL SOFTWARE AND RUNNING IT

1. SETTING UP SYNOPSIS ENVIRONMENT

Check if you have a copy of .tcshrc file in your home directory. If the file already exists, take a back-up of the file and copy the .tcshrc file give on the ECE Computer Support Webpage, else just copy the .tcshrc file into you home directory. Use the following link to access the ECE Computer Support webpage:

<http://www.ece.uic.edu/consulting/index.html>

You can just append the following lines to the end of .tcshrc file if it already exists and donot wish to rewrite it:

```
setenv SYNOPSIS /usr/local/synopsis
setenv LM_LICENSE_FILE 1712@lserver1.ece.uic.edu:1712@lserver2.ece.uic.edu:
1712@lserver3.ece.uic.edu
setenv PATH ${PATH}:${SYNOPSIS}/bin:${SYNOPSIS}/sparcOS5/bin
setenv VCS_HOME /usr/local/synopsis
```

2. DOWNLOAD EXAMPLE SOURCE CODE

Download sample VHDL code given on the website to your home directory under ECE368/src directory.

3. RUNNING SYNOPSIS VHDL SOFTWARE (Written by Hasan Arslan)

To compile and simulate the vhd code, please follow the steps described below. The source code should be copied into the src directory under ECE368 directory.

Compiling **ckt1.vhd** :

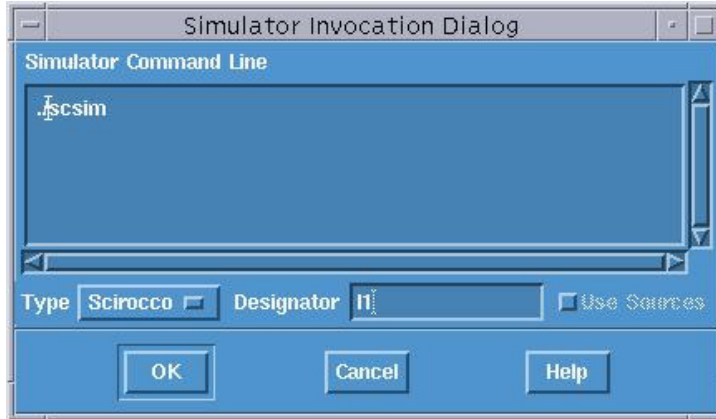
1. Go to ECE368/sim directory
2. Type **vhdlan ../src/ckt1.vhd** at the command prompt and press enter. If it gives any error message about c compiler or CS_CCPTH make sure that you have **/usr/local/bin** in your PATH. To check it type **echo \$PATH**. If it is not defined in your PATH please add it.
3. To compile vhd design, type (at the prompt):
scs <entity_name> <architecture of entity>. In ckt1.vhd, the entity define is ckt1 and its architecture type is behav. So type **scs ckt1 behav** to compile the design entity.
The compiler will create an executable file named **scsim**. Type **ls** to see the file.
4. Synopsis VHDL software includes a graphical user interface called Scirocco which allows us to debug the VHDL code and perform post-simulation analysis.
Type in the following command to invoke scirocco:

```
scirocco &
```

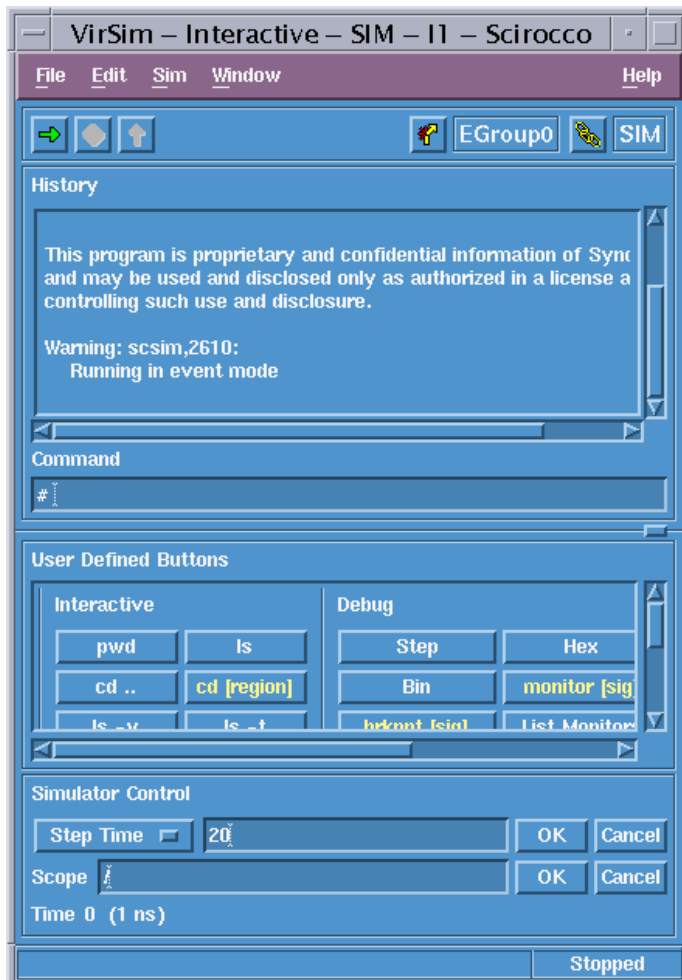
The & will run scirocco as a background process in your login session.

A window to invoke the simulator will start after a few seconds. In the Simulation Command Line box, scsim is already typed. Add a ./ before scsim and press OK. The command should look like this:

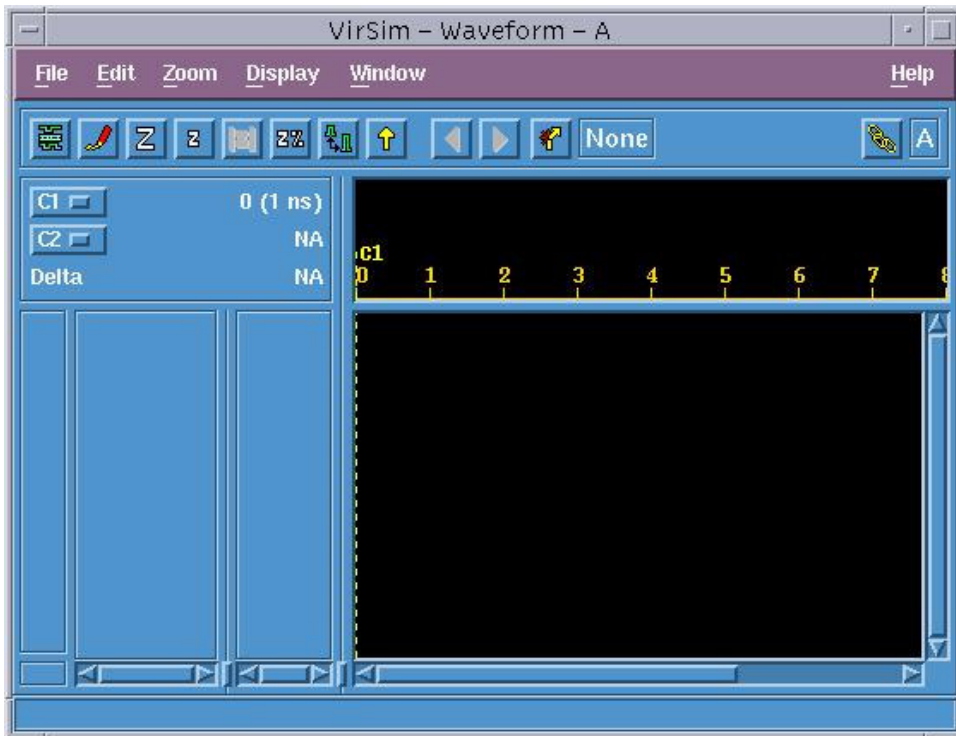
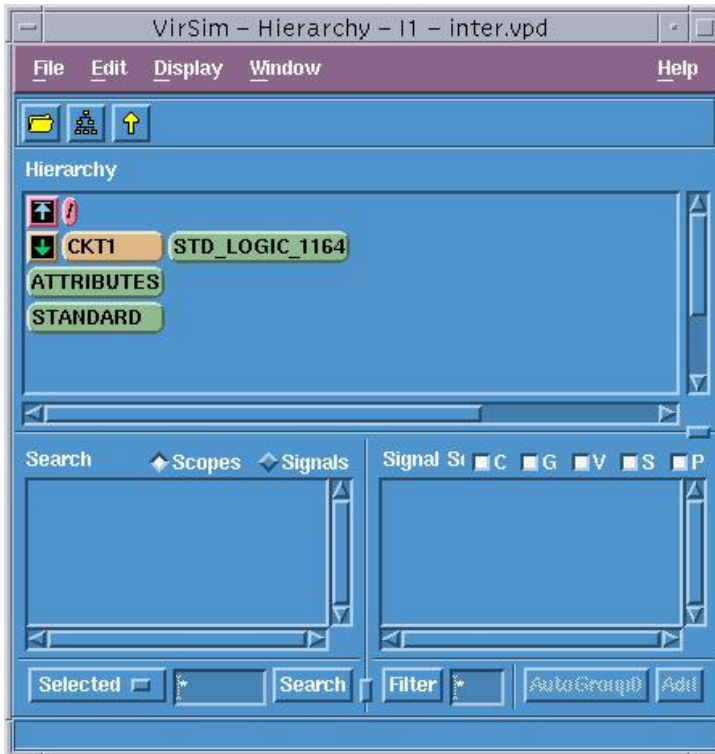
```
./scsim
```



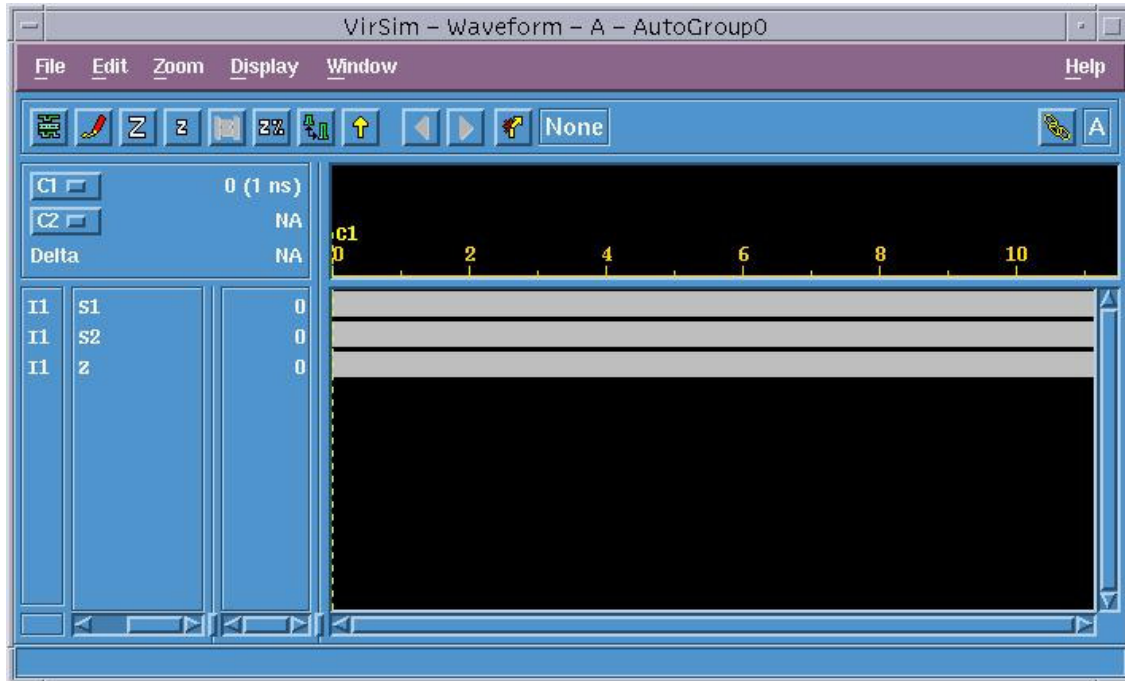
5. The interactive <VirSim> simulation window appears as shown below.



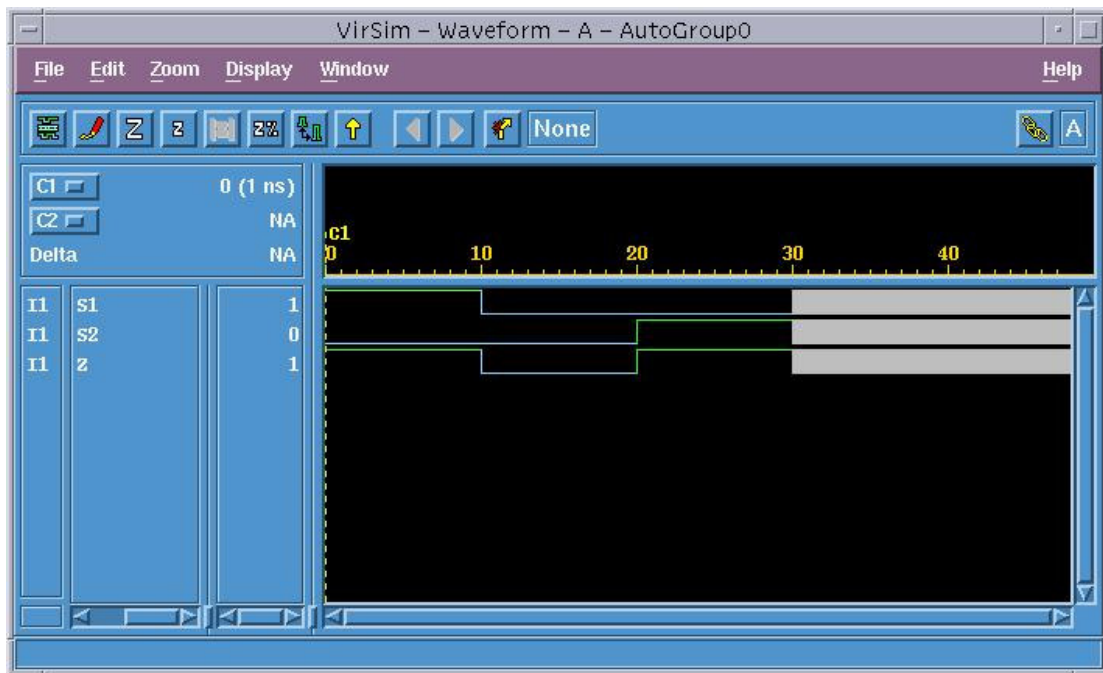
6. On the Virsim GUI, click the Hierarchy and Waveform buttons. The Hierarchy window and Waveform window should appear.



7. In the Hierarchy window, left click **CKT1**. Left click a signal you want to look at under Signal Select. Using the middle mouse button, drag the signal over the Waveform window. Repeat this for every signal you would like to view and analyze.



8. In order to assign values to the signals, you have to be on the same hierarchy level as the included signals. Therefore type the command **cd ckt1** (similar to the UNIX commands, cd, ls, etc) in the <VirSim Interactive> window Command pane. In order to see all signals on the actual hierarchy level just click on ls in the User Defined Buttons area. Now use the command-**assign** to assign a first value to s1, **assign '1' s1** and press enter. Give also a value to the s2 by typing **assign '0' s2**.
9. Run the simulation for 10 ns by entering run 10 in the command pane.
10. Assign a logical '0' to the s1 signal and run the simulation for another 10 ns. In order to see the whole simulation, use zoom option.
11. Assign a logical '1' to the s2 signal and run the simulation for another 10 ns.



Repeat step 11 by assigning different values to input signals.

12. In the Waveform window, select File --> Print. You can specify the begin time and end time of the final print out and the print command is `lpr -Picl4`

Compile **ckt2.vhd**:

1. Go to ECE368/sim directory
2. type `vhdlan ../src/ckt2.vhd` and press enter.
3. `scs ckt1 data_flow`
 ckt2.vhd uses the same entity definition ckt1, but uses a different architecture name which is data_flow.
4. Repeat steps 4-12 described above to get the simulation results. Only name of the signals will be different.

For Compiling a structural vhd code, we need to do some extra step before getting results. First, compile all components that have been used in the structural description of an entity and then we have to compile main entity. Ckt3.vhd file presents a structural VHDL design example.

Compiling ckt3.vhd:

1. Go to ECE368/sim directory
2. Type `vhdlan ../src/and_gate.vhd` and press enter.
3. Type `vhdlan ../src/or_gate.vhd` and press enter.
4. Type `vhdlan ../src/not_gate.vhd` and press enter.
5. Type `vhdlan ../src/ckt3.vhd` and press enter.
6. scs ckt1 structure (ckt3.vhd has the same entity name)
7. Repeat steps 4-12 described for ckt1.vhd. Only name of the signals will be different.

Using test bench:

A test bench is used to automate the process of assigning inputs to the input ports for testing and debugging a VHDL design. ckt_tb.vhd test bench file can be used for all three vhd code without doing any changes.

Using test bench file for ckt1.vhd.

1. Go to ECE368/sim directory
2. Type `vhdlan ../src/ckt1.vhd` and press enter.
3. Type `vhdlan ../src/ckt_tb.vhd` and press enter
4. `scs ckt_tb structure`
5. repeat steps 4-10 which is explained for ckt1.vhd. This time don't assign any value to a signal.(if you assign it will give error message). Just run the simulation entering `run` in the command pane . Simulation will be stopped after 40 ns.

Using test bench file for ckt2.vhd.

1. Go to ECE368/sim directory
2. Type `vhdlan ../src/ckt2.vhd` and press enter.
3. Type `vhdlan ../src/ckt_tb.vhd` and press enter
4. `scs ckt_tb structure`
5. Repeat steps 4-10 which is explained for ckt1.vhd at top. This time don't assign any value to a signal.(if you assign it will give error message). Just run the simulation entering `run` in the command pane . Simulation will be stopped after 40 ns.

Using test bench file for structural architecture definition.

1. Go to ECE368/sim directory
2. Type `vhdlan ../src/and_gate.vhd` and press enter.
3. Type `vhdlan ../src/or_gate.vhd` and press enter.
4. Type `vhdlan ../src/not_gate.vhd` and press enter.
5. Type `vhdlan ../src/ckt3.vhd` and press enter.
6. Type `vhdlan ../src/ckt_tb.vhd` and press enter
7. `scs ckt_tb structure`
8. Repeat steps 4-10 which is explained for ckt1.vhd at top. This time don't assign any value to a signal.(if you assign it will give error message). Just run the simulation entering `run` in the command pane . Simulation will be stopped after 40 ns.