

ECE 368, Fall 2006, Instructor: Prof. Shantanu Dutt

Final Exam: Tue, Dec. 12, Time: 1-3 pm

Exam Format: Open book with only text and 2 pages of notes

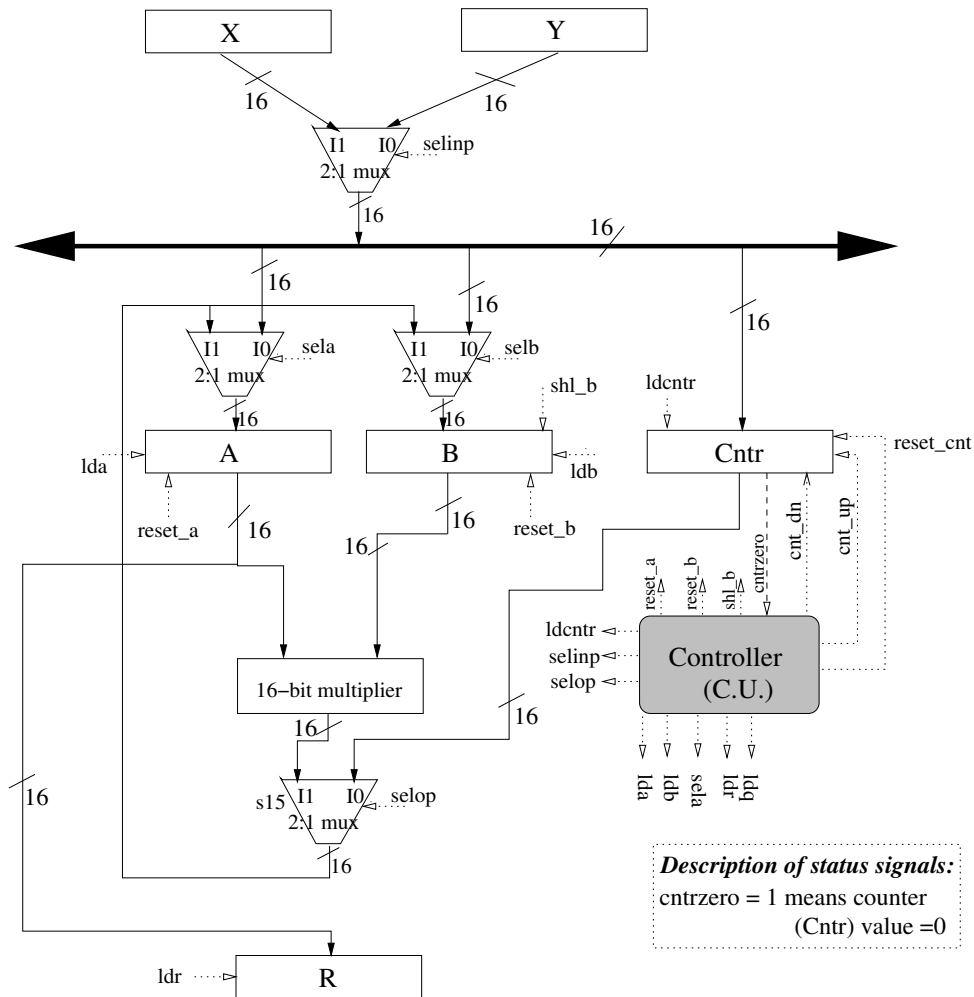
Total Points: 100

Important Note: (1) Write your name on the top of this question sheet and submit along with your answer book

(2) You need to show all your work **clearly** in deriving the answers. Just writing down the final answers is not enough.

Suggestion: Begin by reading all questions and do those first that you think you know best.

1. Digital Design – Datapath Control



Description of status signals:
 cntzero = 1 means counter (Cntr) value = 0

Description of control signals:

lda = 1 means load/write A	sela controls i/p conn. Mux to reg. A	cnt_up = 1 means Cntr ← Cntr + 1
reset_a = 1 means A ← 0	= 0 means I0 inp. conn. to A	cnt_dn = 1 means Cntr ← Cntr - 1
ldb = 1 means load/write B	= 1 means I1 inp. conn. to A	reset_cnt = 1 means Cntr ← 0
reset_b = 1 means B ← 0	selb, selinp, selop also control	ldcntr = 1 means load/write Cntr
shl_b = 1 means contents of B	Muxes and have similar interpretation of their 0/1 values	ldr = 1 means load/write R
are shifted left by 1 bit		

NOTE: All write/cnt up operations complete only at the +ve edge of the next cc (since they all load new values into regs)
 NOTE: Signal lines without any specified width are 1-bit wide

(a) For the datapath shown on the previous page, design the Moore state diagram of the FSM for the control unit that executes the following function in the datapath described below using regular programming language statements:

```

begin
A=1; B=X; Cntr=Y; /* X, Y are positive integers */
while (Cntr > 0) do begin
A = A*B; Cntr=Cntr-1;
endwhile
R=A;
end

```

IMPORTANT NOTES:

- Not all control signals may be needed for executing the above function.
- Using the datapath, you need to determine a way to get the integer value 1 in the A register before beginning to execute the **while** loop.
- The multiplier is a combinational or parallel multiplier, not the sequential add-and-shift multiplier discussed in class.
- Assume that all operations in the datapath except multiply takes 1 cc, and multiply takes 3 cc's.
- Assume that the multiplication operation in each step produces an output representable in 16 bits.
- State beside each state of your FSM the RTL description of what is being accomplished in that state.

You will be graded most importantly on the correctness of your FSM controller, and then on the speed and number of states of your design. **40**

(b) What function of X and Y is stored at the end in R? Illustrate with an example. **7**

(c) Determine the delay in cc's as a function of Y, that your FSM controller takes to execute the above function. **8**

2. VHDL Coding

A 1-to- 2^k demultiplexor (demux) has one input I (of say, n bits) and 2^k outputs $O_0, O_1, \dots, O_{2^k-1}$ (each of n bits). It has a k -bit select input S , and an enable input en . Its functionality is that if $en = 1$ then $O_j = I$ if the integer value represented by S is j and all other $O_m = 0$ for $m \neq j$. Otherwise, if $en = 0$, then all $O_m = 0, 0 \leq m \leq 2^k - 1$.

Give the entity and behavioral architectural description of this demux with generic parameters k and n (of type `natural`). Assume the inputs I and S are bit vectors. Also assume the availability of a function `bitvec2int(X, t)` that converts a t -bit `bit_vector` X to an integer. Finally, note that if X and Y are two vectors of the same type and length, you can do assignments like $X := Y$ if X is a *variable* and $X \leftarrow Y$ if X is a *signal*.

Write your code clearly and with appropriate comments to aid understanding.

25

3. Division Algorithms

Assume that add/sub takes 3 cc's and shift-left takes 1 cc. Also assume that besides add/sub and shift-left both *restoring* and *non-restoring* division require 1 cc for initialization (outside the iteration loop) and that non-restoring division requires a shift-left and at most one subtract operation **after** the iteration loop. Restoring division does **not** require any step after the iteration loop.

For 16-bit division, determine showing clear derivation steps the number of cc's required by (i) restoring and (ii) non-restoring division algorithms when the resulting quotient Q will be

1101101001111010

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