

# ECE 366 - Computer Architecture

Fall 2001

MWF 10:00-10:50 pm, F3 LC

## Teaching Staff

Instructor: Professor Shantanu Dutt, 355-1314, 930 SEO  
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Instructor's Office Hours: Mon 11:15am-12:45pm, Wed 3:00-4:30 pm

**Course web page:** <http://www.ece.uic.edu/~dutt/ece366/ece366.html>  
Check this web page daily for important messages and announcements, and general information.

Teaching Assistant: TBA

## Course Materials

1. Texts:
  - 1) D. Patterson and H. Hennesey, "Computer Organization and Design: The Hardware/Software Interface", Morgan Kaufmann, San Mateo, California, 2nd Ed., 1998.
  - 2) Mythsim manual extracted from: Solworth - Computer Organization Manuscript. This manual will be made available in the library reserve desk for you to copy.
2. Lecture notes will be made available on-line (see course web page) and sometimes in the library.

## Homework Assignments

Five homeworks and two projects will be assigned. These are due before the beginning of the class period on the due date; no homeworks will be accepted after class starts. Solutions will be made available. **Late homework will not be accepted.**

Graded homework will be brought to class by the TA.

## Examination Schedule

NOTE: All exams will be closed book and closed notes. No make-up exams will be given except in extreme circumstances like a serious health problem that is documented and verifiable beforehand (not after the fact).

Fri Oct. 19—tentative, in class

**Final Exam: During Finals week—to be announced**

## Grading System

Homework	20%
Midterm	20%
Projects 1 & 2	20%
Final Exam	40%

## Course Outline

1. **Introduction:** computer organization and architecture—what these terms mean, MIPS instruction set (lecture notes + parts of Chap. 3).
2. **Review of FSM Design:** Moore and Mealy machines (lecture notes)
3. **Processor Datapath:** instruction execution path, arithmetic logic unit (ALU), register files, memory interface, pipelining, performance metrics. Datapaths for the myth8 and the MIPS processors will be discussed. (Chap. 5, parts of Chap. 6, lecture notes, myth8 manual)
4. **Control Unit (CU) Design:** FSM description and design of CUs, hardwired and firmwired CUs (Chap. 5, lecture notes)
5. **Computer Arithmetic:** addition, multiplication, division, high-speed arithmetic units (mainly lecture notes; similar discussion in Chap. 4).
6. **Memory organization:** memory technology, memory hierarchy, associative memories, caches, AMAT metric (mainly lecture notes; similar discussion in Chap. 7).
7. **Input/Output:** (if time permits) communication and synchronization mechanisms between independent modules, various I/O organizations, direct memory access (DMA), bus structures (parts of Chap. 8)

### Assumed Background—Very Important

Please revise your background thoroughly in the topics below, which you covered in your pre-req courses. This is required for you in order to comprehend the material in this course and to do well in homeworks and exams.

1. **Number Systems and Codes** (Secs. 4.1 and 4.2).
2. **Logic Design—Combinational and Sequential Circuit Design, Latches, FFs** (Appendix B excluding the discussions on PLAs, ROMs, SRAMs, DRAMs and Asynchronous Inputs and Synchronizers).
3. **Computer Assembly Language** (given partly in Chap. 3).