

EECS 366, Fall 99, Instructor: Shantanu Dutt

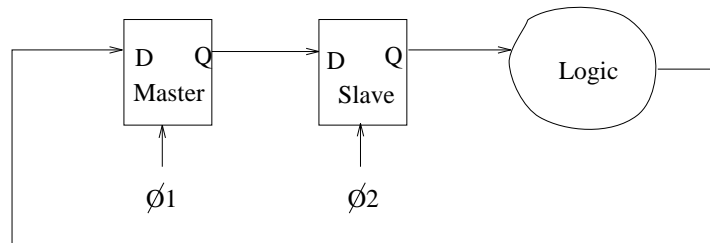
Midterm Exam: Fri., Oct. 15, Time: class time (50 mins)

Exam Format: Closed Book, Total Points: 70

Important Note: You need to show all your work **clearly** in deriving the answers. Just writing down the final answers is not enough.

Suggestion: Begin by reading all questions and do those first that you think you know best.

1. Consider the following 1-bit master-slave combination of level sensitive D-FFs controlled by non-overlapping clocks ϕ_1, ϕ_2 with a feedback path through a logic circuit:



- (a) Can the Master FF be written more than once with different data during ϕ_1 high period? Why or why not? 7
- (b) Can the Slave FF be written more than once with different data during ϕ_2 high period? Why or why not? 8
2. We saw the following control program for the [blt r_j r_k rel_addr] instruction for myth8 in class:

1. $rj_{sel}, rk_{sel}, alu_{sel} = SUB, c_{in}$,
if m_7 then goto negative else goto positive endif;
2. negative: $rj_{sel}, rk_{sel}, alu_{sel} = SUB, c_{in}$,
if v then goto fetch else goto branchlt endif;
3. positive: $rj_{sel}, rk_{sel}, alu_{sel} = SUB, c_{in}$,
if v then goto branchlt else goto fetch endif;
4. branchlt: $result_{sel} = IR_CONST4, r6_{write}$;
5. $a_{sel} = 7, b_{sel} = 6, alu_{sel} = ADD, r7_{write}$,
goto fetch;

Rewrite the control program so that the number of states required to implement this instruction reduces from 5 to 4. Briefly explain your strategy. The myth8 processor organization is provided later in this question sheet. **15**

3. Explain using basics of 2's complement arithmetic, why the following control statement correctly tests if register r_3 is equal to zero? **10**

1. $a_{sel} = 3, alu_{sel} = SUBA,$

if c_{out} then goto r3-nonzero else goto r3-zero;

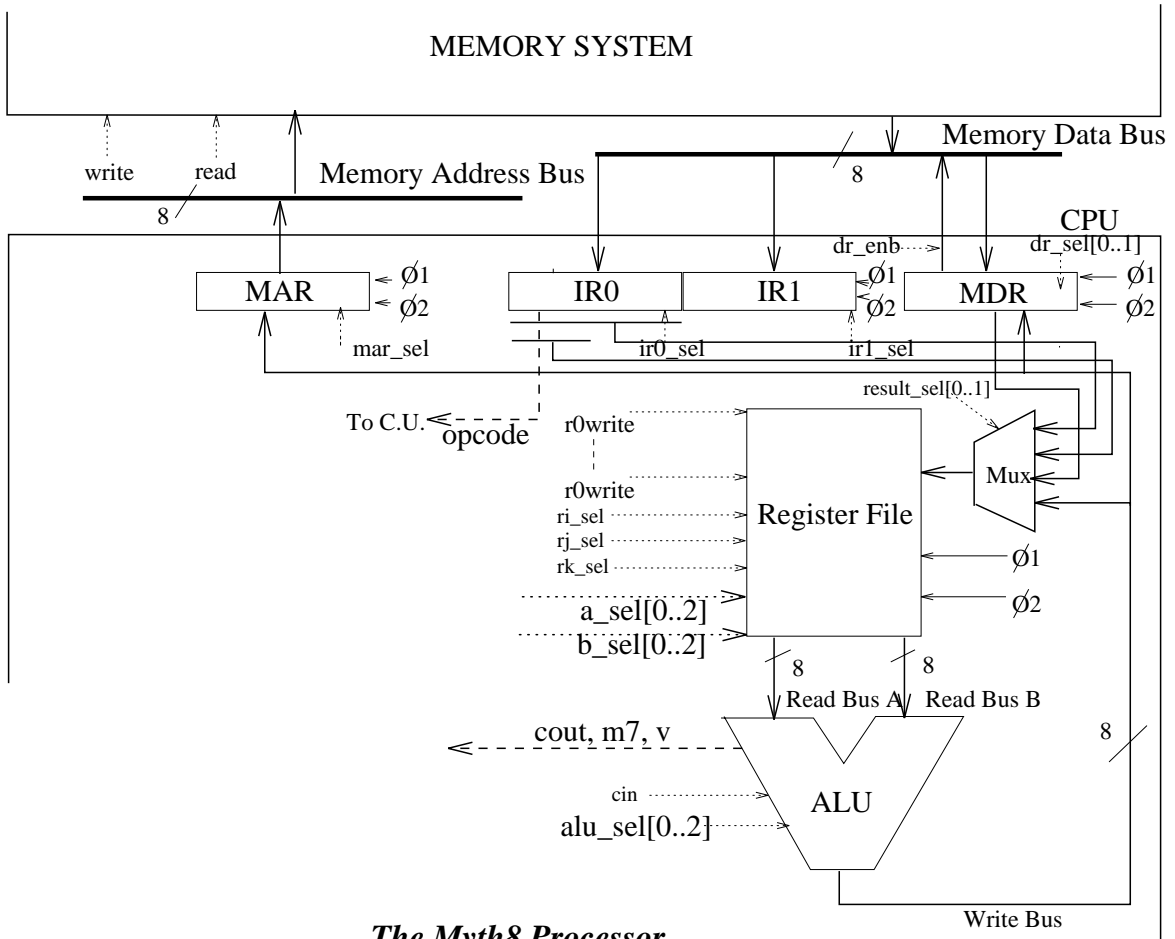
4. Draw a Moore FSM for that part of the control unit of the myth8 processor that performs the following conditional load given by:

$[load\ eq\ r_i\ r_j\ r_k\ rel_addr]$. The semantics of this instruction is $r_i \leftarrow MEM[r_7 + rel_addr]$ if $r_j = r_k$.

You need to only provide the states after the decode state of the myth8 control unit.

All relevant control signal values need to be shown in each state (they can be given symbolically like $alu_{sel} = SUB, dr_{sel} = MEM, result_{sel} = MDR, dr_{sel} = ALU$, etc. to mean obvious operations; explain what your control signal symbols mean). If appropriate, you can show transitions from the state(s) you design to a "Fetch" state without giving details of the Fetch state. The myth8 processor organization is provided on the next page. **30**

Hint: Can be done in 5 states. If you do this correctly using more than 5 states you will get partial credit, but this will decrease linearly with every extra state (beyond 5).



The Myth8 Processor