

ECE 366—Fall 2001, Instructor: Prof. Shantanu Dutt

Homework 1 : Due Wed Sept. 5

Some problems below are FSM design problems, and are intended to help you revise your background on this topic from EECS 265. You can refer to any of several Logic Design texts for this including those by Mano, Katz, Hayes, etc. A solid background in sequential circuits is very important for this course. For the FSM design problems **always**: (1) Indicate the *reset* state; (2) Label each state symbolically to indicate what “information” the state represents and/or what it does.

1. **(Instruction Flow)** Using the base figures of a datapath and control in Lecture Notes # 3, and a scheme similar to that shown in the notes for the ADD instruction, illustrate (using PowerPoint generated figures) the sequence of microinstructions that the processor will execute for the following instructions:

(a) [lw r_i 16-bit_offset_addr] — Semantics: $r_i \leftarrow \text{MEM}[\text{PC} + 16\text{-bit_offset_addr}]$.

Note that 16-bit_offset_addr is a 16-bit immediate field in the instruction. **40**

(b) [jump 24-bit_offset_addr] — Semantics: $\text{PC} \leftarrow \text{PC} + 24\text{-bit_offset_addr}$. **40**

Assume that the memory data and address buses are 32 bits; hence all registers including the PC is also 32 bits. Add any necessary connections and logic (registers, FUs, Muxes, etc.) at a high level (just like in the current figures) over and above those in the Lecture Notes # 3 figure in order to execute this load instruction.

Hint: You need another register for storing the address of a word to be loaded from memory (generally called the *memory address register* or MAR). The MAR is then connected to the mem. address bus for getting the desired word into the register file. Note that the PC and IR are used for instruction fetch purposes only, not for fetching data.

2. **(Register File Design)** In class we saw the design of a register file with only one write port. In some advanced processors, two different registers in the register file may need to be written simultaneously from different sources. Thus register files with two write ports are desirable. Note that the write ports are only ports at the register file level not at the register/FF level (registers/FFS have only one input line or one input “port”). Assume for this design that the two destination registers will always be different (it does not make sense to write the same dest. register from two different sources simultaneously!).

Design a register file with positive edge-triggered clocking, with 4 registers in it (you can show each register as a rectangle; no need to show FFs in it) with two write ports connected to two write buses WB_A and WB_B , so that two different registers can be written simultaneously, one from each bus. Show all components that you need (Muxes, Tristate logic, Decoders etc) clearly and show all relevant control signals used to control the writing into the registers. Explain clearly your design and the functions of the control signals. **60.**

NOTE & Hint: Each register is composed of D-FFs, which have only one input each; thus each register has one input finally coming into it. You cannot assume that each FF has 2 data inputs for the convenience of your design task. The idea is to be able to steer one of the write bus inputs to the desired register using suitable logic units. For e.g., if we need to perform $r_2 \leftarrow WB_A; r_5 \leftarrow WB_B$, then your design should simultaneously steer the data on WB_A to r_2 's input and the data on WB_B to r_5 's input (plus do other things so that these data get written to r_2 and r_5 , etc.).

3. **(Review material: FSM)**

A sequential circuit has one input (X) and one output (Z). Draw a Mealy FSM's STD if $Z = 1$ if and only if the total number of 1's received on X is divisible by 3 or 5 (e.g., 0, 3, 5, 6, 10, ...).

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4. **(Review material: FSM)**

A sequential circuit has two inputs and two outputs. The inputs X_1, X_2 represent a 2-bit binary number, N . If the present value of N is less than the previous value, then $Z_1 = 1$. If the present value of N is less than the previous value, then $Z_2 = 1$. Otherwise, Z_1 and Z_2 are 0. Derive:

(a) A Mealy machine STD (**Hint:** Only 5 states are needed).

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(b) A Moore FSM's STD (**Hint:** At least 11 states are needed).

NOTE: In contrast to a Mealy FSM, in a Moore FSM, the output depends only on the current state, and thus the output in the STD is NOT associated with transition arcs, but is associated with the states.

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